PAW3395DM-T6QU: Optical Gaming Navigation Chip

General Description

PAW3395DM-T6QU is PixArt Imaging's new low power high end gaming navigation chip with illumination source in a 16-pin molded lead-frame DIP package. It provides best in class gaming experience with the enhanced features of high speed, high resolution, high accuracy and selectable lift detection height to fulfill professional gamers' need. It is designed to be used with LM19-LSI or L0AE-LSI1 to achieve optimum performance.

Key Features

- Low power consumption of typical 1.7 mA in run mode (HP Mode)
- 16-pin molded lead-frame DIP package with 850nm illumination source
- Enhanced programmability
  - Gaming Mode
    - High Performance Mode (HP Mode)
    - Low Power Mode (LP Mode)
    - Corded Gaming Mode
  - Lift detection options
    - 1mm and 2mm setting
    - Manual lift cut off calibration
- Selectable resolutions up to 26000 cpi with 50 cpi step size
- Angle snapping
- Angle tunability
- Resolution error of 0.4% (typical) at 5000cpi on QCK up to 200ips
- High speed motion detection 650ips* and acceleration 50g*
- Self–adjusting variable frame rate for optimum performance
- Internal oscillator — no clock input needed
- 4-wire serial port interface (SPI)
- Motion interrupt output

Applications

- Corded and cordless optical gaming mice
- Integrated input devices

Key Parameters

Parameter	Value
Power supply Range	VDD: 1.8 to 2.1V VDDIO: 1.8 to 3.3V
Lens Magnification	1:1
Interface	4-wire Serial Port Interface
Typical Operating Current @ VDD = 1.9V **Note:** includes LED current	Run: 1.7 mA (HP Mode) Run: 1.3 mA (LP Mode) Rest1: 580 µA Rest2: 11 µA Rest3: 6 µA Power Down: 4 µA
Resolution	Up to 26000 cpi
Tracking Speed	650* ips
Acceleration	50* g
Dimension size (package assemble with LM19-LSI lens)	10.90 x 16.20 x 9.81 mm^3

Note: * - HP Mode

Ordering Information

Part Number	Description	Package Type	Packing Type	MOQ
PAW3395DM-T6QU	Optical Gaming Navigation Chip	16-pin DIP	Tube	1,000
LM19-LSI	Round Lens	Round Lens	Tray	1,000
L0AE-LSI1	Trim Lens	Trim Lens	Tray	1,000

RoHS compliant

For any additional inquiries, please contact us at http://www.pixart.com

Table of Content

PAW3395DM-T6QU: Optical Gaming Navigation Chip 1
General Description 1
Key Features 1
Applications 1
Key Parameters 1
Ordering Information 1
Table of Content 2
List of Figures 4
List of Tables 5
1.0 Introduction 6
1.1 Chip Overview 6
1.2 Pin Configuration 7
2.0 Electrical Specifications 8
2.1 Regulatory Requirements 8
2.2 Absolute Maximum Ratings 8
2.3 Recommended Operating Conditions 9
2.4 AC Electrical Specifications 10
2.5 DC Electrical Specifications 12
3.0 Mechanical Specifications 13
3.1 Chip Package Dimension 13
3.2 Package Marking 13
3.3 Chip Assembly Drawings 14
3.4 Lens Assembly Drawings 15
3.4.1 Assembly with LM19-LSI Lens 15
3.4.2 Assembly with L0AE-LSI1 Lens 16
3.5 PCB Assembly Recommendations 17
3.6 Packing Information 18
3.6.1 Packing Tube 18
3.7 Package Handling Information 19
3.7.1 Sample of Inner Box Label 19
3.7.2 Sample of Shipping Box Label 19
4.0 Reference Schematics 20
5.0 Serial Peripheral Interface (SPI) 21
5.1 Signal Description 21
5.2 Motion Pin Timing 21
5.3 Chip Select Operation 21
5.4 Write Operation 22
5.5 Read Operation 23
5.6 Required Timing Between Read and Write Commands (tsxx) 24
5.7 Burst Mode Operation 25
5.7.1 Motion Read 25
5.7.2 Procedure to Start Motion Burst 26
6.0 Power-up Sequence 27

6.1 Power on Sequence 27
6.2 Power-Up Initialization Register Setting 27
6.3 NRESET 29
7.0 Operation Guides 30
7.1 RawData Output 30
7.2 Shutdown 32
7.3 Gaming and Office Mode Setting 33
7.4 Universal Lift Cut Off 35
7.5 Manual Lift Cut Off Calibration 35
7.5.1 Lift Cut off Calibration Procedures 35
7.5.2 Enable Lift Cut off Calibration Register Setting 37
7.5.3 Disable Lift Cut off Calibration Register Setting 37
7.6 Power Management for Wireless Mode 38
8.0 Registers 39
8.1 Registers Summary Table 39
8.2 Registers Description 40
8.3 Bit Masks for Register Write 54
Revision History 55

List of Figures

Figure 1. Block Diagram 6
Figure 2. Device Pinout 7
Figure 3. Packages Outline Drawing 13
Figure 4. Recommended Chip Orientation, Mechanical Cutouts and Spacing (Top View) 14
Figure 5. Exploded View of Assembly with LM19-LSI Lens 15
Figure 6. Exploded View of Assembly with L0AE-LSI1 16
Figure 7. Packing Tube 18
Figure 8. Reference Schematic Diagram 20
Figure 9. Write Operation 22
Figure 10. MOSI Setup and Hold Time 22
Figure 11. Read Operation 23
Figure 12. MISO Delay and Hold Time 23
Figure 13. Timing Between Two Write Commands 24
Figure 14. Timing Between Write and Either Write or Subsequent Read Commands 24
Figure 15. Timing Between Read and Either Write or Subsequent Read Commands 24
Figure 16. Motion Read Sequence 26
Figure 17. RawData Map (Surface Referenced) 31

List of Tables

Table 1. Pin Definition 7
Table 2. Absolute Maximum Ratings 8
Table 3. Recommended Operating Condition 9
Table 4. AC Electrical Specifications 10
Table 5. DC Electrical Specifications 12
Table 6. Package Marking Description 13
Table 7. Recommended R_{LED} 20
Table 8. SPI Port Signals Description 21
Table 9. State of Signal Pins After VDD is Valid 29
Table 10. Pin Status in Shutdown Mode 32
Table 11. Rest Modes Response and Downshift Time 38

1.0 Introduction

1.1 Chip Overview

PAW3395DM-T6QU is an optical navigation chip targeted for high-end cordless and corded gaming mouse. It contains a picture element array as Image Acquisition System (IAS), a Digital Signal Processor (DSP), a 4-wire serial port, a power control circuit and built-in LED driver integrated with IR LED in a package as shown in the block diagram. The chip measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values. An external microcontroller reads the Δx and Δy information from the chip serial port. The microcontroller then translates the data into USB, or RF signals before sending them to the host PC or game console.

Notes: Throughout this document PAW3395DM-T6QU is referred as the chip.

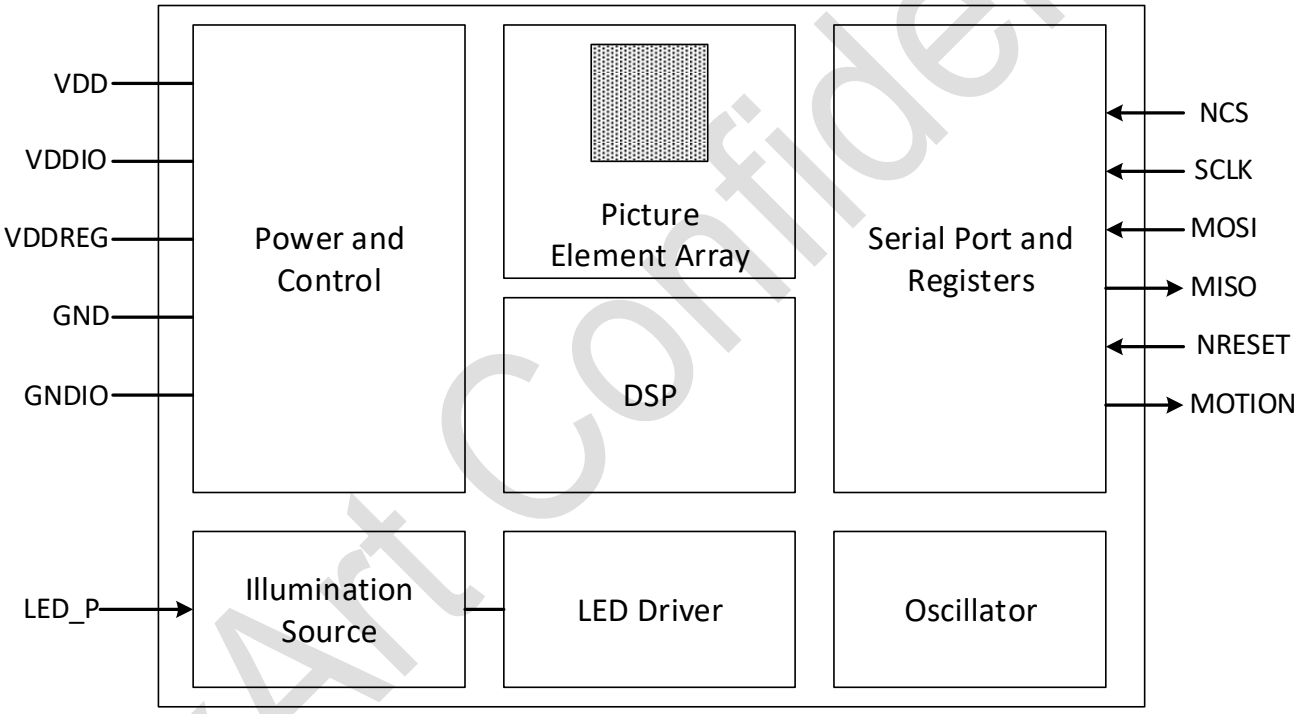


Figure 1. Block Diagram

1.2 Pin Configuration

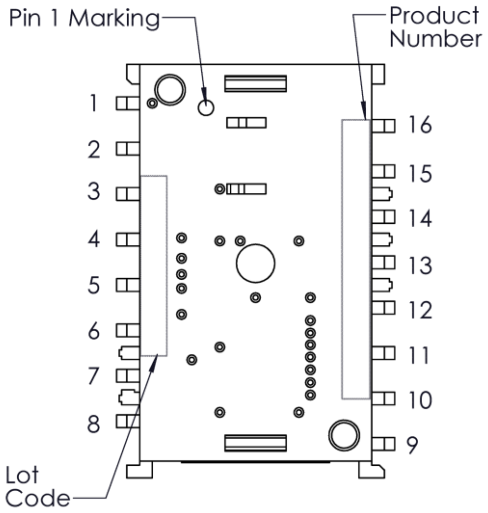


Figure 2. Device Pinout

Table 1. Pin Definition

Pin No.	Function	Symbol	Type	Description
1	Reserved	NC	NC	No connection
2	Reserved	NC	NC	No connection
3	Supply Ground	GND	Ground	Ground
4	Supply Voltage	VDD	Power	Input power supply
5	LDO Output	VDDREG	Power	LDO output for digital core (only for internal usage)
6	Reserved	NC	NC	No connection
7	I/O Voltage	VDDIO	Power	I/O power supply
8	I/O Ground	GNDIO	Ground	I/O Ground
9	Motion Output	MOTION	Output	Motion detect
10	4-wire SPI	SCLK	Input	Serial data clock
11		MOSI	Input	Serial data input
12		MISO	Output	Serial data output
13		NCS	Input	Chip select (Active Low)
14	Reset Control	NRESET	Input	Chip reset (Active Low)
15	LED	LED_P	Input	LED Anode
16	Reserved	NC	NC	No connection

2.0 Electrical Specifications

2.1 Regulatory Requirements

- Passes FCC "Part15, Subpart B, Class B", "ICES-003:2016 Issue 6, Class B" and "ANSI C63.4:2014" when assembled into a mouse with shielded USB cable using ferrite bead and following PixArt's recommendations.
- Passes IEC 62471: 2006 Photo biological safety of lamps and lamp systems.

2.2 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temperature	T_{SOLDER}		260	°C	For 7 seconds, 1.6mm below seating plane
Supply Voltage	VDD	-0.5	2.1	V	
	VDDIO	-0.5	3.3	V	
ESD	ESDHB		2	kV	Human Body Model on all pins
Input Voltage	V_{IN}	-0.5	3.3	V	All I/O pins

Notes:

1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.

2.3 Recommended Operating Conditions

Table 3. Recommended Operating Condition

Parameter	Symbol	Min	Typ.	Max	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	VDD	1.8	1.9	2.1	V	Excluding supply noise
	VDDIO	1.8	1.9	3.3	V	Excluding supply noise. (VDDIO must be the same or greater than VDD)
Power Supply Rise Time	t_{RT}	0.15		20	ms	0 to VDD min
Supply Noise peak to peak	V_{NA}			100	mV	10 kHz —75 MHz
Serial Port Clock Frequency	f_{SCLK}			10	MHz	50% duty cycle
Distance from Lens Reference Plane to Tracking Surface	Z	2.2	2.4	2.6	mm	
Speed ▪ High Performance Mode ▪ Low Power Mode ▪ Corded Gaming Mode ▪ Office Mode	S	 650 480 650 200			ips	In run mode at 45 degree
Acceleration ▪ High Performance Mode ▪ Low Power Mode ▪ Corded Gaming Mode ▪ Office Mode	A	 50 40 50 10			g	
Resolution Error ▪ High Performance Mode ▪ Low Power Mode ▪ Corded Gaming Mode	Res_{Err}		 0.4 0.4 0.4		%	Up to 200ips on QCK at 5000cpi
Lift Cutoff 1mm setting	$Lift_{1mm}$		1		mm	PixArt standard gaming surface
Lift Cutoff 2mm setting	$Lift_{2mm}$		2		mm	PixArt standard gaming surface

2.4 AC Electrical Specifications

Table 4. AC Electrical Specifications

Chip electrical characteristics over recommended operating conditions. Typical values are at 25°C, VDD = 1.9V and VDDIO=1.9V

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Motion Delay After Reset	$t_{MOT-RST}$	50			ms	From reset to valid motion, assuming motion is present
Shutdown	t_{STDWN}			500	ms	From Shutdown mode active to low current
Wake from Shutdown	t_{WAKEUP}	50			ms	From Shutdown mode inactive to valid motion. **Notes:** A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown"
MISO Rise Time	t_{r-MISO}		6		ns	C_L = 20pF
MISO Fall Time	t_{f-MISO}		6		ns	C_L = 20pF
MISO Delay After SCLK	$t_{DLY-MISO}$			35	ns	From SCLK falling edge to MISO data valid C_L = 20pF
MISO Hold Time	$t_{hold-MISO}$	25			ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	25			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	25			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte
SPI Time Between Write and Read Commands	t_{SWR}	5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte
SPI Time Between Read and Subsequent Commands	t_{SRW} t_{SRR}	2			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command
SPI Read Address-Data Delay	t_{SRAD}	2			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer

Parameter	Symbol	Min	Typical	Max	Unit	Notes
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK-NCS}$	1			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS To MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r-MOTION}$		300		ns	C_L = 20pF
MOTION Fall Time	$t_{f-MOTION}$		300		ns	C_L = 20pF
Input Capacitance	C_{in}		10		pF	SCLK, MOSI, NCS
Load Capacitance	C_L			20	pF	MISO, MOTION
Transient Supply Current	I_{DDT}			70	mA	Max supply current during the supply ramp from 0V to V_{DD} with min 150 µs and max 20ms rise time. (Does not include charging currents for bypass capacitors)
	I_{DDTIO}			60	mA	Max supply current during the supply ramp from 0V to V_{DDIO} with min 150 µs and max 20ms rise time. (Does not include charging currents for bypass capacitors)

2.5 DC Electrical Specifications

Table 5. DC Electrical Specifications

Chip electrical characteristics over recommended operating conditions. Typical values are at 25°C, VDD = 1.9V, VDDIO = 1.9V, and with LED current at 50mA.

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
DC Supply Current (High Performance Mode)	IDD_{RUN} IDD_{REST1} IDD_{REST2} IDD_{REST3}		1.7 580 11 6		mA µA µA µA	Up to 200ips ▪ IDD_{RUN} : Average current consumption, including LED current with 1ms polling ▪ IDD_{REST} : Average current consumption, including LED current
DC Supply Current (Low Power Mode)	IDD_{RUN} IDD_{REST1} IDD_{REST2} IDD_{REST3}		1.3 580 11 6		mA µA µA µA	Up to 200ips ▪ IDD_{RUN} : Average current consumption, including LED current with 1ms polling ▪ IDD_{REST} : Average current consumption, including LED current
DC Supply Current (Corded Gaming Mode)	IDD_{RUN}		10		mA	Up to 650ips IDD_{RUN} : Average current consumption, including LED current with 0.125ms polling
DC Supply Current (Office Mode)	IDD_{RUN} IDD_{RUN} IDD_{REST1} IDD_{REST2} IDD_{REST3}		0.6 0.4 70 11 6		mA mA µA µA µA	Up to 200ips Up to 30ips ▪ IDD_{RUN} : Average current consumption, including LED current with 8ms polling ▪ IDD_{REST} : Average current consumption, including LED current
Shutdown Current	IPD		4		µA	
Input Low Voltage	V_{IL}			0.3xVDDIO	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7xVDDIO			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{leak}		±1	±10	µA	V_{in}=VDDIO or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{out} = 1mA for MISO I_{out} = 0.1mA for MOTION
Output High Voltage	V_{OH}	VDDIO -0.45			V	I_{out} = -1mA for MISO I_{out} = -0.1mA for MOTION

3.0 Mechanical Specifications

This section covers chip's guidelines and recommendations in term of chip, lens & PCB assemblies.

3.1 Chip Package Dimension

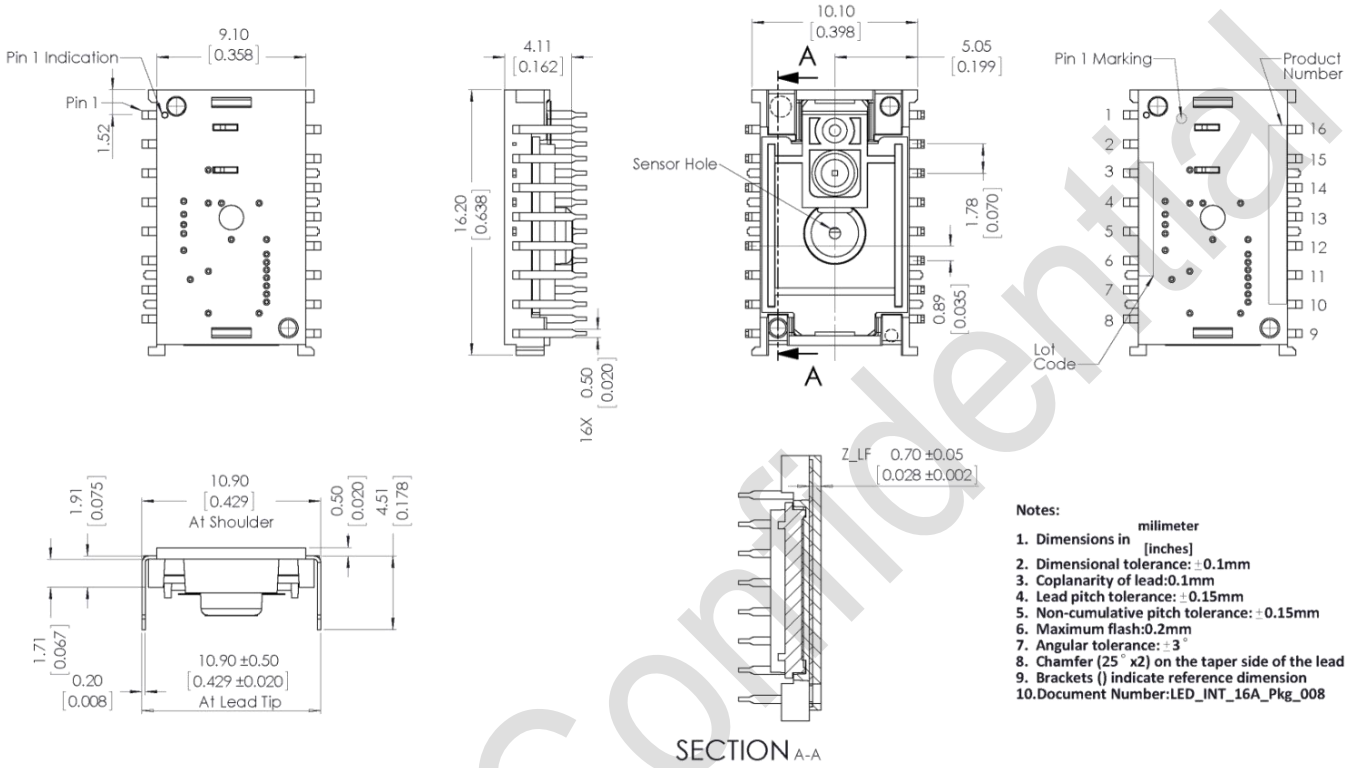


Figure 3. Packages Outline Drawing

CAUTION: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

3.2 Package Marking

Table 6. Package Marking Description

Items	Marking	Remark
Product Number	PAW3395DM-T6QU	
Lot Code	AYWWXXXXX	A: Assembly house Y: Year WW: Week XXXXX: PixArt reference

3.3 Chip Assembly Drawings

It is highly recommended to follow the chip orientation in Figure 4 to achieve optimum tracking performance.

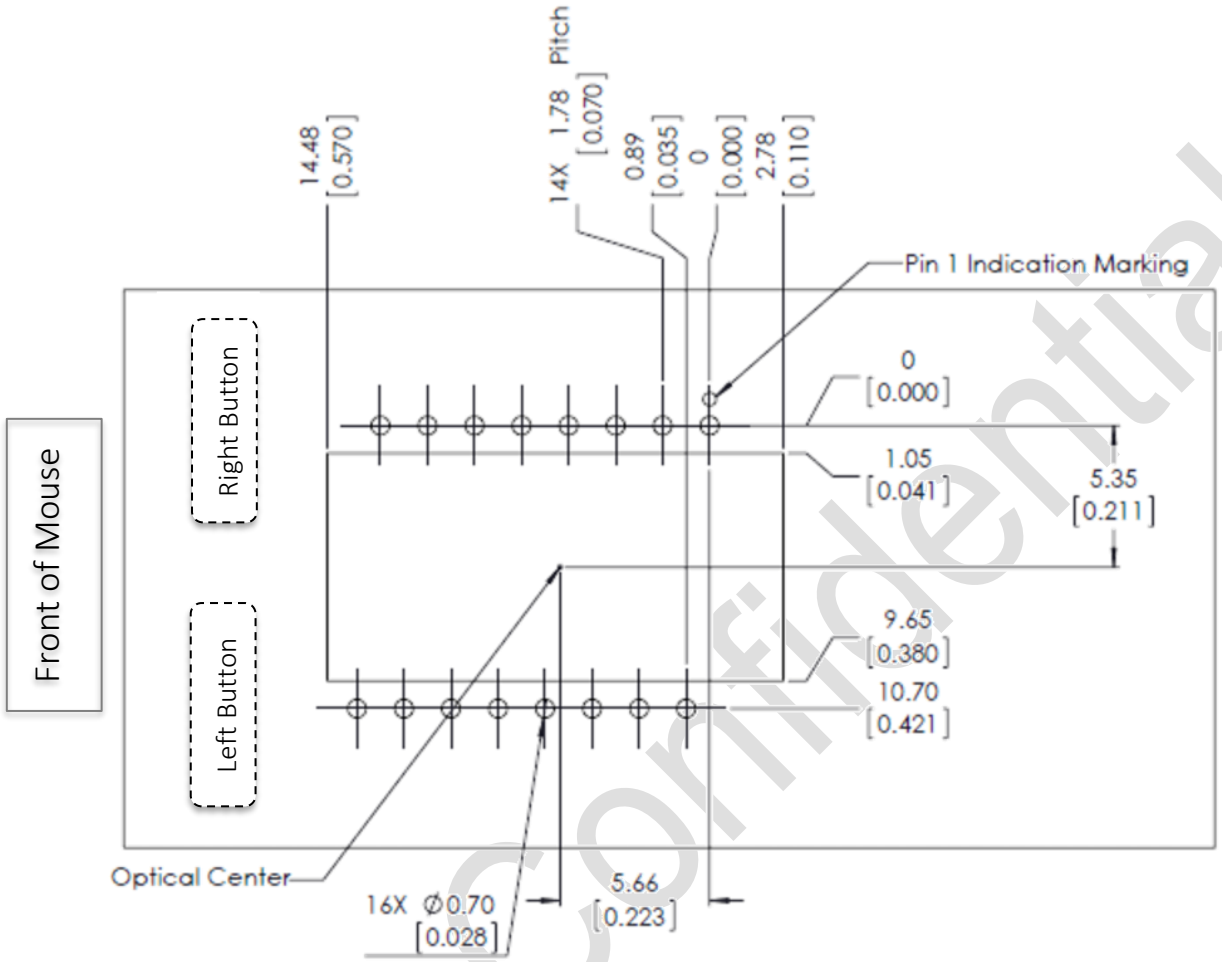


Figure 4. Recommended Chip Orientation, Mechanical Cutouts and Spacing (Top View)

3.4 Lens Assembly Drawings

3.4.1 Assembly with LM19-LSI Lens

Refer to the LM19-LSI lens datasheet for the detail.

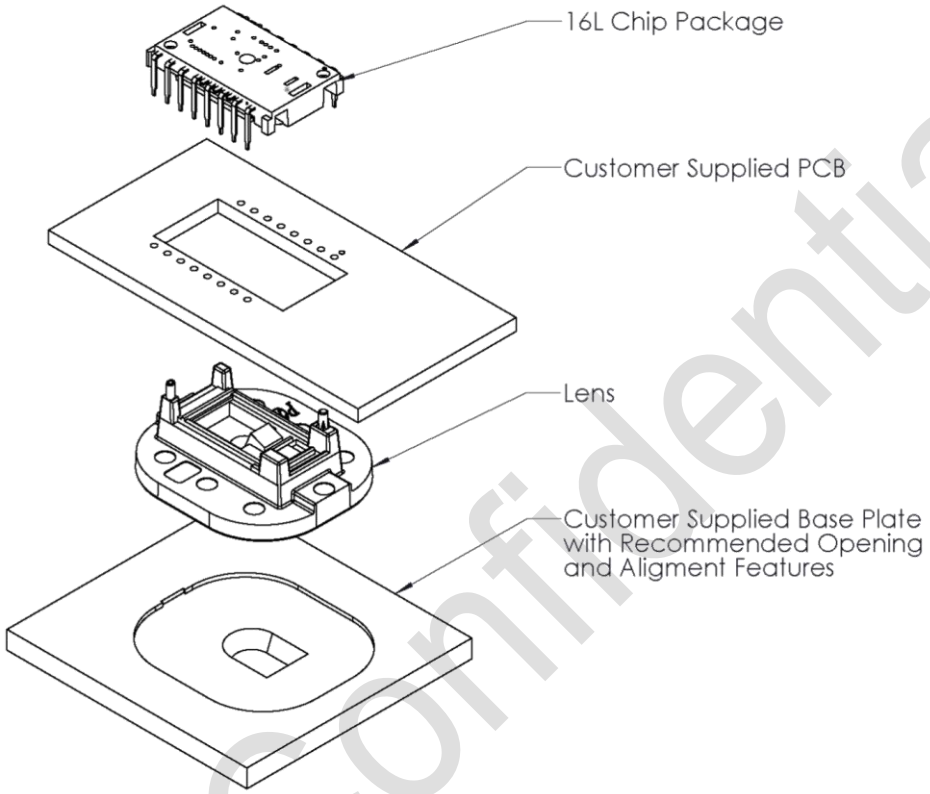


Figure 5. Exploded View of Assembly with LM19-LSI Lens

3.4.2 Assembly with L0AE-LSI1 Lens

Refer to the L0AE-LSI1 lens datasheet for the detail.

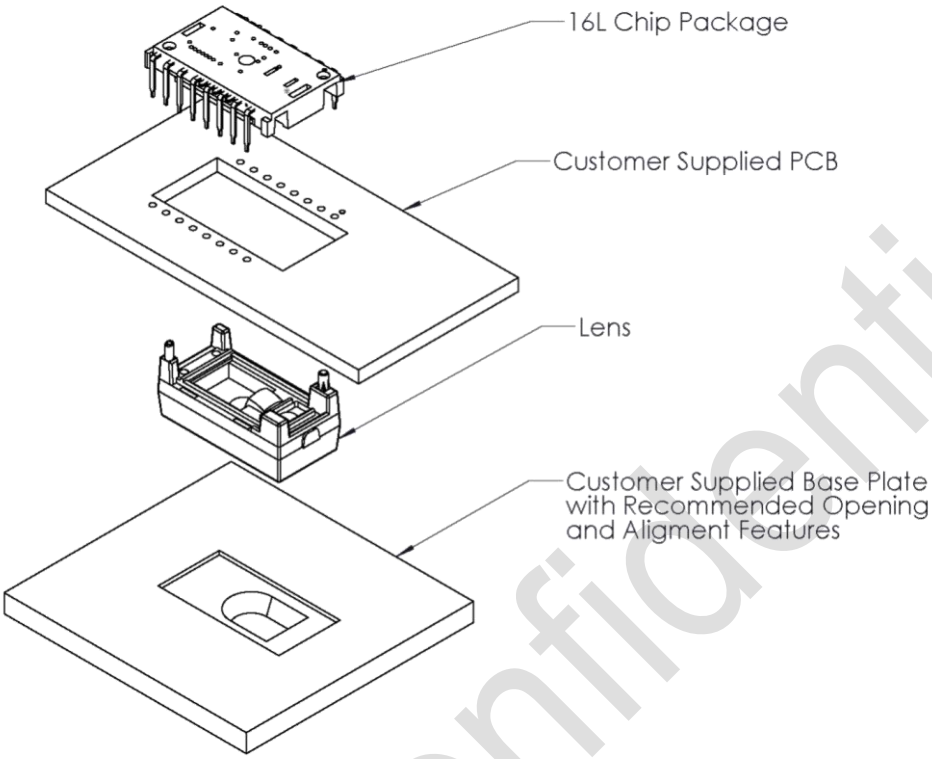


Figure 6. Exploded View of Assembly with L0AE-LSI1

3.5 PCB Assembly Recommendations

1. Insert the integrated chip and all other electrical components into PCB.
2. Wave-solder the entire assembly in a no-wash solder process utilizing solder-fixture. A solder-fixture is required to protect the chip from flux spray and wave solder paste.
3. Avoid getting any solder flux onto the chip body as there is potential for flux to seep into the chip package, the solder fixture should be designed to expose only the chip leads to flux spray & molten solder while shielding the chip body and optical apertures. The fixture should also set the chip at the correct position and height on the PCB.
4. Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.
5. Remove the protective Kapton tapes from optical apertures of the chip. Care must be taken to prevent contaminants from entering the apertures. Do not place the PCB with the chip facing up during the entire mouse assembly process. Hold the PCB vertically when removing Kapton tape.
6. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The chip package will self-align to the lens via the guide posts. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
7. Recommendation: The lens can be permanently secured to the chip package by melting the lens' guide posts over the chip with heat staking process. Please refer to Application Note titled "LM19-LSI Lens: PCB Assembly & Lens Heat Staking Recommendations" for details and recommendation on the lens heat staking process.
8. Install mouse top case. There must be a feature in the top case to press down onto the PCB assembly to ensure all components are stacked or interlocked to the correct vertical height.
9. It is recommended to place mouse feet around the base plate opening to stabilize mouse tracking on the surface.

3.6 Packing Information

Item	Description
Product number	PAW3395DM-T6QU
Package type	16L DIP
Quantity per tube	25 pcs
Inner box quantity	1,000 pcs
Shipping box quantity	12,000 pcs
Tube size	500 x 13.5 x 7.0 mm^3
Inner box size	89 x 540 x 58 mm^3
Shipping box size	310 x 560 x 270 mm^3

3.6.1 Packing Tube

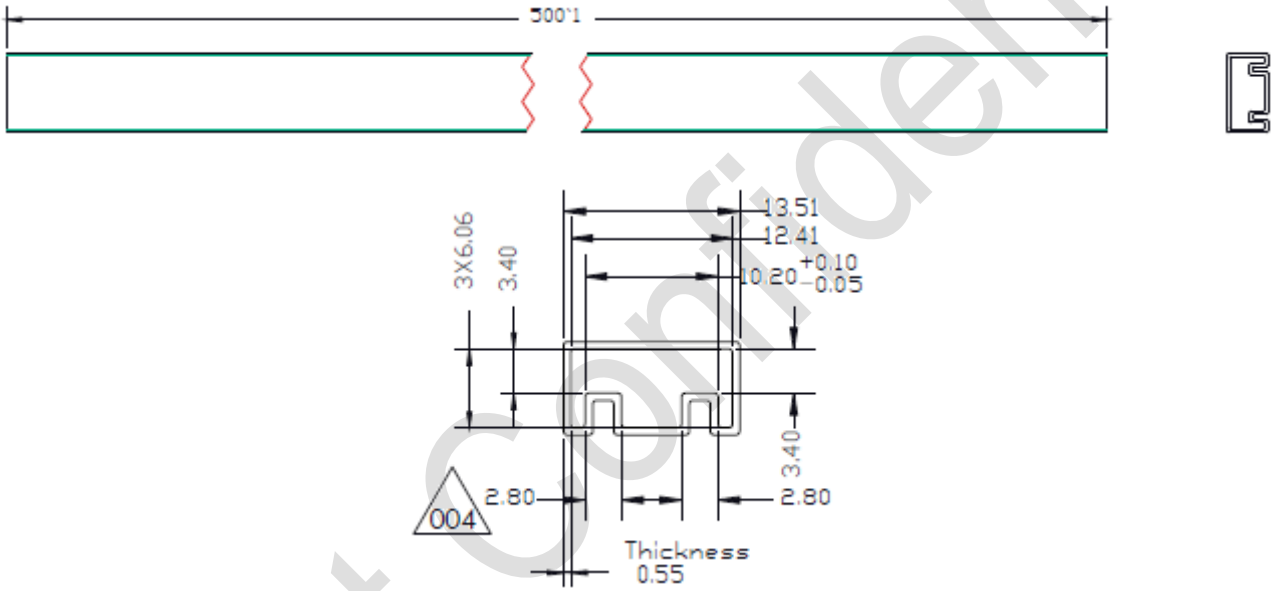
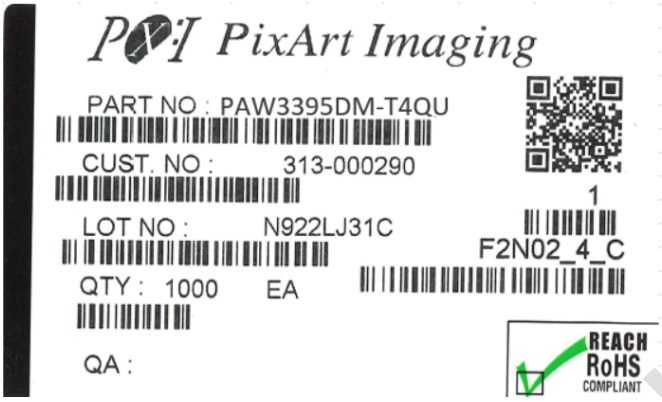


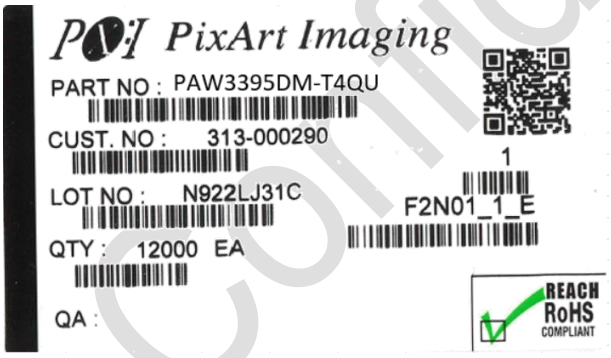
Figure 7. Packing Tube

3.7 Package Handling Information

3.7.1 Sample of Inner Box Label



3.7.2 Sample of Shipping Box Label



4.0 Reference Schematics

It is recommended not to leave the NRESET pin floating, it should be constantly driven by an output pin from the microcontroller to establish its state.

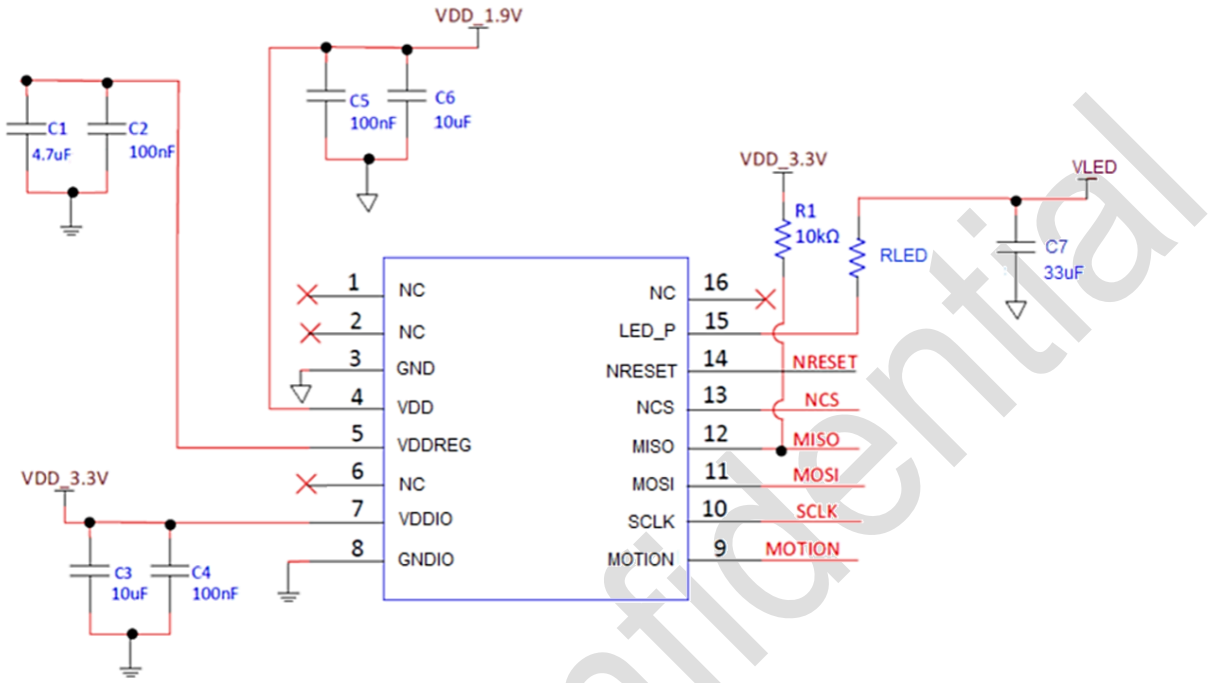


Figure 8. Reference Schematic Diagram

Table 3 shows the recommended value of R_{LED} and V_{LED} to obtain 50mA current for LED. Recommend to use R_{LED} with 1% tolerance.

Table 7. Recommended R_{LED}

VLED (V)	Recommended RLED (Ω)
1.9V	5.6
2.0V	6.8

5.0 Serial Peripheral Interface (SPI)

5.1 Signal Description

The synchronous serial port is used to write and read registers in the chip.

The port is a 4-wire port. The host microcontroller always initiates communication. The chip never initiates any data transfers. SCLK, MOSI and NCS may be driven directly by a microcontroller. The port pins may be shared with other SPI slave devices. When the NCS pin is driven high, the input signals are ignored and the output is tri-stated.

Table 8. SPI Port Signals Description

Signal Name	Functional Description
SCLK	Clock input, generated by the master (microcontroller).
MOSI	Input data. (Master Out/Slave In)
MISO	Output data. (Master In/Slave Out)
NCS	Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

5.2 Motion Pin Timing

The motion pin is an active low output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is non-zero data in the *Delta_X_L, Delta_X_H, Delta_Y_L* or *Delta_Y_H* registers. Clearing the motion bit (by reading *Delta_X_L, Delta_X_H, Delta_Y_L* or *Delta_Y_H* registers) will put the motion pin high.

5.3 Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is required before beginning the next transaction. In order to improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because any ESD and EFT/B event could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete or to terminate burst-mode operation. The port is not available for further use until burst-mode is terminated.

5.4 Write Operation

Write operation, defined as data going from the micro-controller to chip, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The chip reads MOSI on rising edges of SCLK.

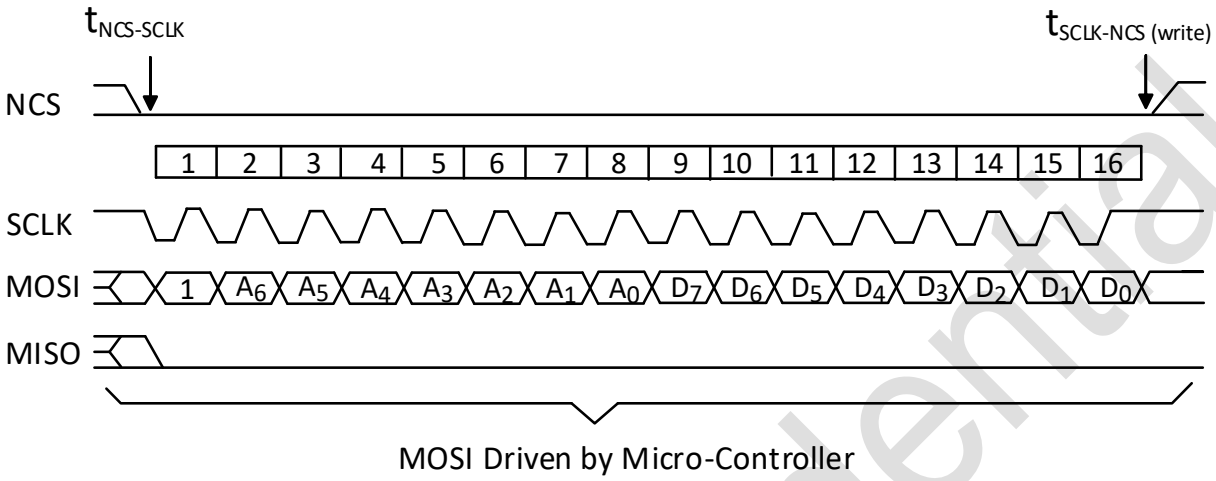


Figure 9. Write Operation

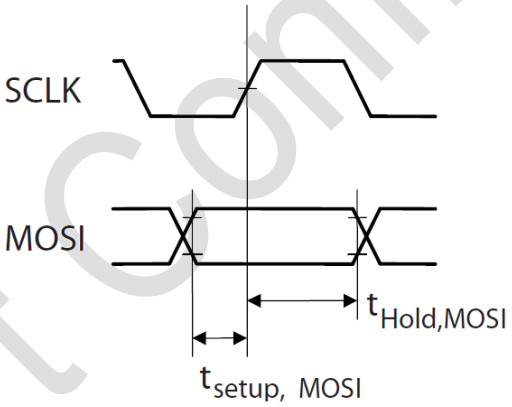


Figure 10. MOSI Setup and Hold Time

5.5 Read Operation

A read operation, defined as data going from chip to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the chip over MISO. The chip outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

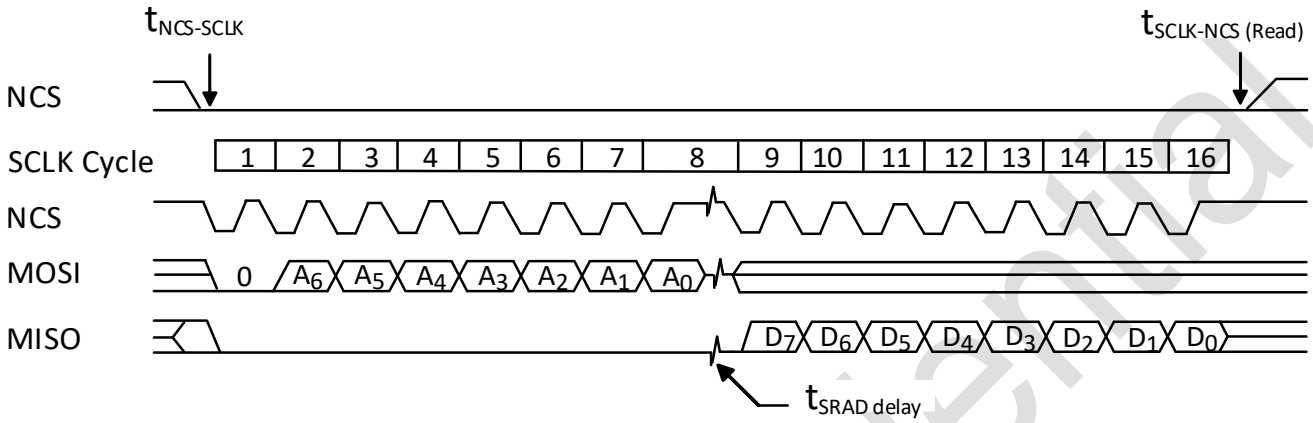


Figure 11. Read Operation

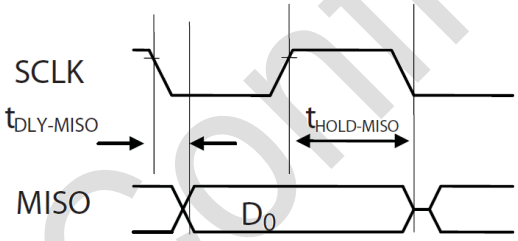


Figure 12. MISO Delay and Hold Time

Note: The minimum high state of SCLK is also the minimum MISO data hold time of the chip. Since the falling edge of SCLK is actually the start of the next read or write command, the chip will hold the state of data on MISO until the falling edge of SCLK.

5.6 Required Timing Between Read and Write Commands (tsxx)

There are minimum timing requirements between read and write commands on the serial port.

If the rising edge of the SCLK for the last data bit of the second write command occurs before the t_{SWW} delay, then the first write command may not complete correctly.

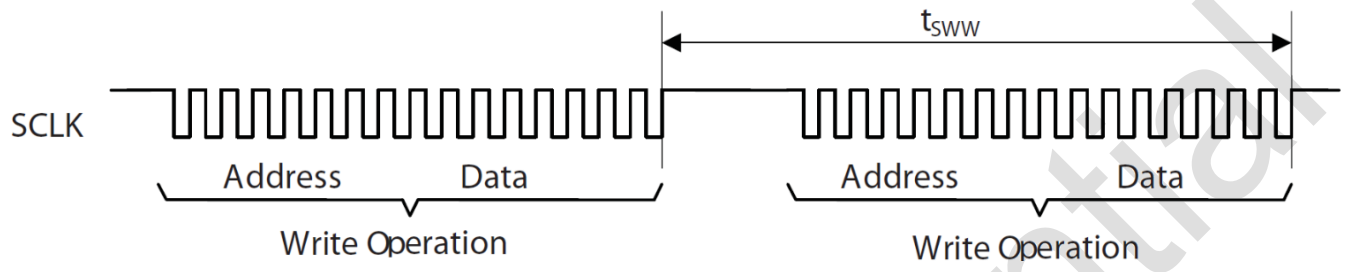


Figure 13. Timing Between Two Write Commands

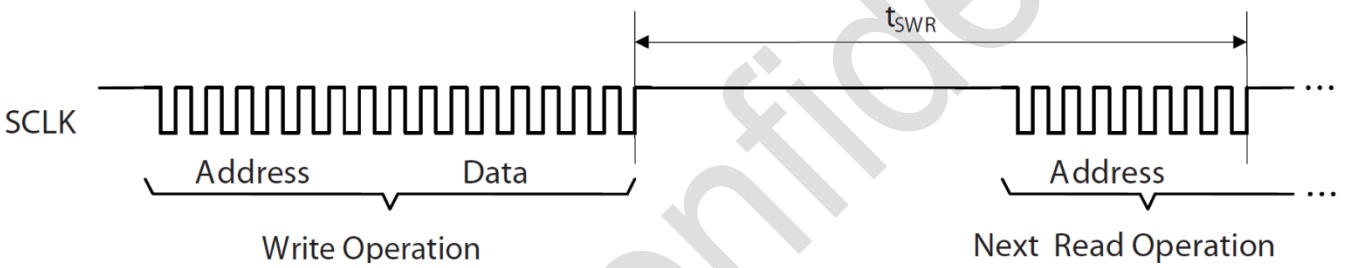


Figure 14. Timing Between Write and Either Write or Subsequent Read Commands

If the rising edge of SCLK for the last address bit of the read command occurs before the t_{SWR} required delay, the write command may not complete correctly. During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the chip has time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that the chip has time to prepare the requested data.

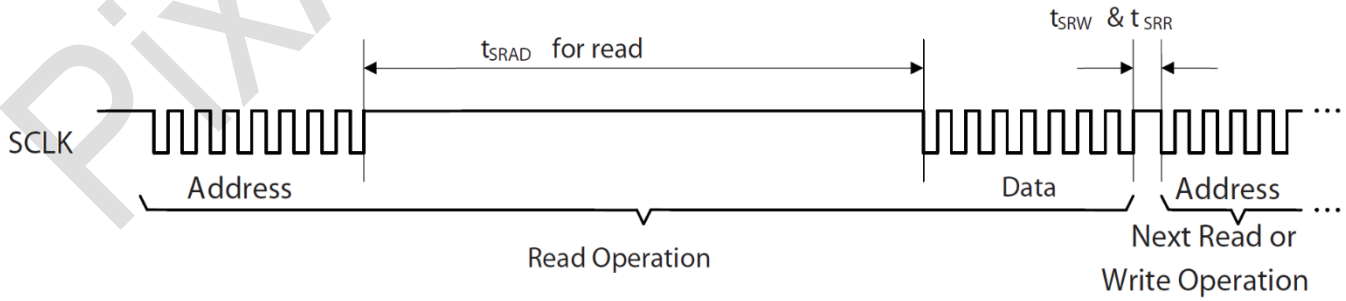


Figure 15. Timing Between Read and Either Write or Subsequent Read Commands

5.7 Burst Mode Operation

Burst mode is a special serial port operation mode which is used to reduce the serial transaction time for predefined registers. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address and by not requiring the normal delay period between data bytes.

5.7.1 Motion Read

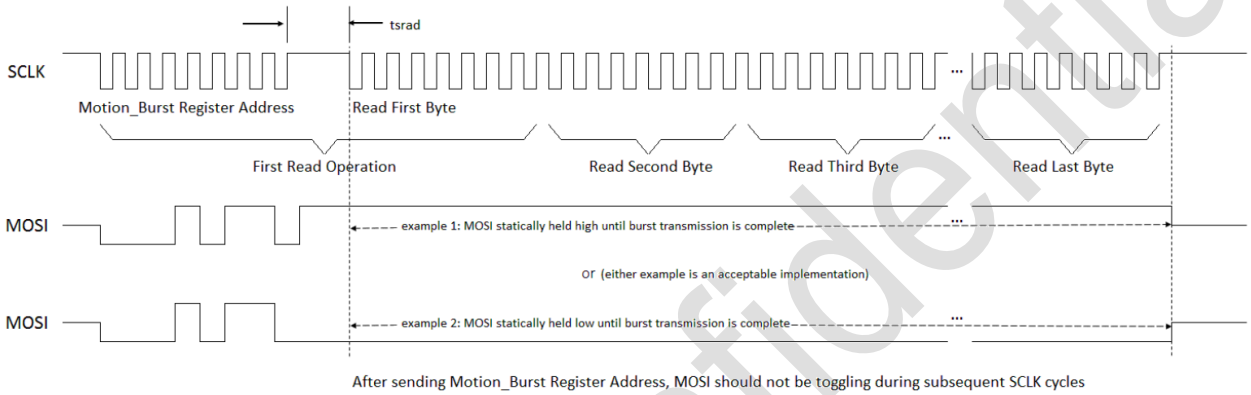
Reading the *Motion_Burst* register activates the Motion Read mode. The chip will respond with the following motion burst report in this order.

BYTE[00] = Motion
BYTE[01] = Observation
BYTE[02] = Delta_X_L
BYTE[03] = Delta_X_H
BYTE[04] = Delta_Y_L
BYTE[05] = Delta_Y_H
BYTE[06] = SQUAL
BYTE[07] = RawData_Sum
BYTE[08] = Maximum_RawData
BYTE[09] = Minimum_Rawdata
BYTE[10] = Shutter_Upper
BYTE[11] = Shutter_Lower

After sending the *Motion_Burst* register address, the microcontroller must wait for t_{SRAD}, and then begins reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data is latched into the output buffer after the last address bit is received. After the burst transmission is complete, the microcontroller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

5.7.2 Procedure to Start Motion Burst

1. Lower NCS.
2. Wait for $t_{NCS-SCLK}$
3. Send *Motion_Burst* address (0x16). After sending this address, MOSI should be held static (either high or low) until the burst transmission is complete.
4. Wait for t_{SRAD}
5. Start reading SPI data continuously up to 12 bytes. Motion burst may be terminated by pulling NCS high for at least t_{BEXIT}.
6. To read new motion burst data, repeat from step 1.



Note: Motion burst data can be read from the *Burst_Motion_Read* register even in run or rest mode. Power-Up Sequences

Figure 16. Motion Read Sequence

6.0 Power-up Sequence

6.1 Power on Sequence

Although the chip performs an internal power up self-reset, it is still recommended that the *Power_Up_Reset* register is written every time power is applied. The recommended chip power up sequence is as follows:

1. Apply power to VDD and VDDIO in any order, with a delay of no more than 100ms in between each supply. Ensure all supplies are stable.
2. Wait for at least 50 ms.
3. Drive NCS high, and then low to reset the SPI port.
4. Write 0x5A to *Power_Up_Reset* register (or alternatively toggle the NRESET pin).
5. Wait for at least 5ms.
6. Load Power-up initialization register setting.
7. Read registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion bit state.

6.2 Power-Up Initialization Register Setting

1. Write register 0x7F with value 0x07
2. Write register 0x40 with value 0x41
3. Write register 0x7F with value 0x00
4. Write register 0x40 with value 0x80
5. Write register 0x7F with value 0x0E
6. Write register 0x55 with value 0x0D
7. Write register 0x56 with value 0x1B
8. Write register 0x57 with value 0xE8
9. Write register 0x58 with value 0xD5
10. Write register 0x7F with value 0x14
11. Write register 0x42 with value 0xBC
12. Write register 0x43 with value 0x74
13. Write register 0x4B with value 0x20
14. Write register 0x4D with value 0x00
15. Write register 0x53 with value 0x0E
16. Write register 0x7F with value 0x05
17. Write register 0x44 with value 0x04
18. Write register 0x4D with value 0x06
19. Write register 0x51 with value 0x40
20. Write register 0x53 with value 0x40
21. Write register 0x55 with value 0xCA
22. Write register 0x5A with value 0xE8
23. Write register 0x5B with value 0xEA
24. Write register 0x61 with value 0x31
25. Write register 0x62 with value 0x64
26. Write register 0x6D with value 0xB8
27. Write register 0x6E with value 0x0F
28. Write register 0x70 with value 0x02
29. Write register 0x4A with value 0x2A
30. Write register 0x60 with value 0x26
31. Write register 0x7F with value 0x06
32. Write register 0x6D with value 0x70
33. Write register 0x6E with value 0x60
34. Write register 0x6F with value 0x04
35. Write register 0x53 with value 0x02
36. Write register 0x55 with value 0x11
37. Write register 0x7A with value 0x01
38. Write register 0x7D with value 0x51
39. Write register 0x7F with value 0x07
40. Write register 0x41 with value 0x10
41. Write register 0x42 with value 0x32
42. Write register 0x43 with value 0x00
43. Write register 0x7F with value 0x08
44. Write register 0x71 with value 0x4F
45. Write register 0x7F with value 0x09
46. Write register 0x62 with value 0x1F
47. Write register 0x63 with value 0x1F
48. Write register 0x65 with value 0x03
49. Write register 0x66 with value 0x03
50. Write register 0x67 with value 0x1F
51. Write register 0x68 with value 0x1F
52. Write register 0x69 with value 0x03
53. Write register 0x6A with value 0x03
54. Write register 0x6C with value 0x1F

55. Write register 0x6D with value 0x1F
56. Write register 0x51 with value 0x04
57. Write register 0x53 with value 0x20
58. Write register 0x54 with value 0x20
59. Write register 0x71 with value 0x0C
60. Write register 0x72 with value 0x07
61. Write register 0x73 with value 0x07
62. Write register 0x7F with value 0x0A
63. Write register 0x4A with value 0x14
64. Write register 0x4C with value 0x14
65. Write register 0x55 with value 0x19
66. Write register 0x7F with value 0x14
67. Write register 0x4B with value 0x30
68. Write register 0x4C with value 0x03
69. Write register 0x61 with value 0x0B
70. Write register 0x62 with value 0x0A
71. Write register 0x63 with value 0x02
72. Write register 0x7F with value 0x15
73. Write register 0x4C with value 0x02
74. Write register 0x56 with value 0x02
75. Write register 0x41 with value 0x91
76. Write register 0x4D with value 0x0A
77. Write register 0x7F with value 0x0C
78. Write register 0x4A with value 0x10
79. Write register 0x4B with value 0x0C
80. Write register 0x4C with value 0x40
81. Write register 0x41 with value 0x25
82. Write register 0x55 with value 0x18
83. Write register 0x56 with value 0x14
84. Write register 0x49 with value 0x0A
85. Write register 0x42 with value 0x00
86. Write register 0x43 with value 0x2D
87. Write register 0x44 with value 0x0C
88. Write register 0x54 with value 0x1A
89. Write register 0x5A with value 0x0D
90. Write register 0x5F with value 0x1E
91. Write register 0x5B with value 0x05
92. Write register 0x5E with value 0x0F
93. Write register 0x7F with value 0x0D
94. Write register 0x48 with value 0xDD
95. Write register 0x4F with value 0x03
96. Write register 0x52 with value 0x49
97. Write register 0x51 with value 0x00
98. Write register 0x54 with value 0x5B
99. Write register 0x53 with value 0x00
100. Write register 0x56 with value 0x64
101. Write register 0x55 with value 0x00
102. Write register 0x58 with value 0xA5
103. Write register 0x57 with value 0x02
104. Write register 0x5A with value 0x29
105. Write register 0x5B with value 0x47
106. Write register 0x5C with value 0x81
107. Write register 0x5D with value 0x40
108. Write register 0x71 with value 0xDC
109. Write register 0x70 with value 0x07
110. Write register 0x73 with value 0x00
111. Write register 0x72 with value 0x08
112. Write register 0x75 with value 0xDC
113. Write register 0x74 with value 0x07
114. Write register 0x77 with value 0x00
115. Write register 0x76 with value 0x08
116. Write register 0x7F with value 0x10
117. Write register 0x4C with value 0xD0
118. Write register 0x7F with value 0x00
119. Write register 0x4F with value 0x63
120. Write register 0x4E with value 0x00
121. Write register 0x52 with value 0x63
122. Write register 0x51 with value 0x00
123. Write register 0x54 with value 0x54
124. Write register 0x5A with value 0x10
125. Write register 0x77 with value 0x4F
126. Write register 0x47 with value 0x01
127. Write register 0x5B with value 0x40
128. Write register 0x64 with value 0x60
129. Write register 0x65 with value 0x06
130. Write register 0x66 with value 0x13
131. Write register 0x67 with value 0x0F
132. Write register 0x78 with value 0x01
133. Write register 0x79 with value 0x9C
134. Write register 0x40 with value 0x00
135. Write register 0x55 with value 0x02
136. Write register 0x23 with value 0x70
137. Write register 0x22 with value 0x01
138. Wait for 1ms

139. Read register 0x6C at 1ms interval until value 0x80 is obtained or read up to 60 times, this register read interval must be carried out at 1ms interval with timing tolerance of ±1%

    If value of 0x80 is not obtained from register0x6C after 60 times:

    a. Write register 0x7F with value 0x14
    b. Write register 0x6C with value 0x00
    c. Write register 0x7F with value 0x00

140. Write register 0x22 with value 0x00
141. Write register 0x55 with value 0x00
142. Write register 0x7F with value 0x07
143. Write register 0x40 with value 0x40
144. Write register 0x7F with value 0x00

During power-up there will be a period of time after the power supply is high but before normal operation. The table below shows the state of the various pins during power-up and reset.

Table 9. State of Signal Pins After VDD is Valid

Pin	During Reset	After Reset
NRESET	Functional	Functional
NCS	Ignored	Functional
MISO	Undefined	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
MOTION	Undefined	Functional

6.3 NRESET

The NRESET pin is used to perform the chip full chip reset. When asserted, it performs the same reset function as the *Power_Up_Reset_*Register. The NRESET pin needs to be asserted (held to logic 0) for at least 100 ns duration for the chip to reset.

Note: NRESET pin has a built in weak pull up circuit. During active low reset phase, the NRESET pin can draw a static current of up to 600µA.

7.0 Operation Guides

7.1 RawData Output

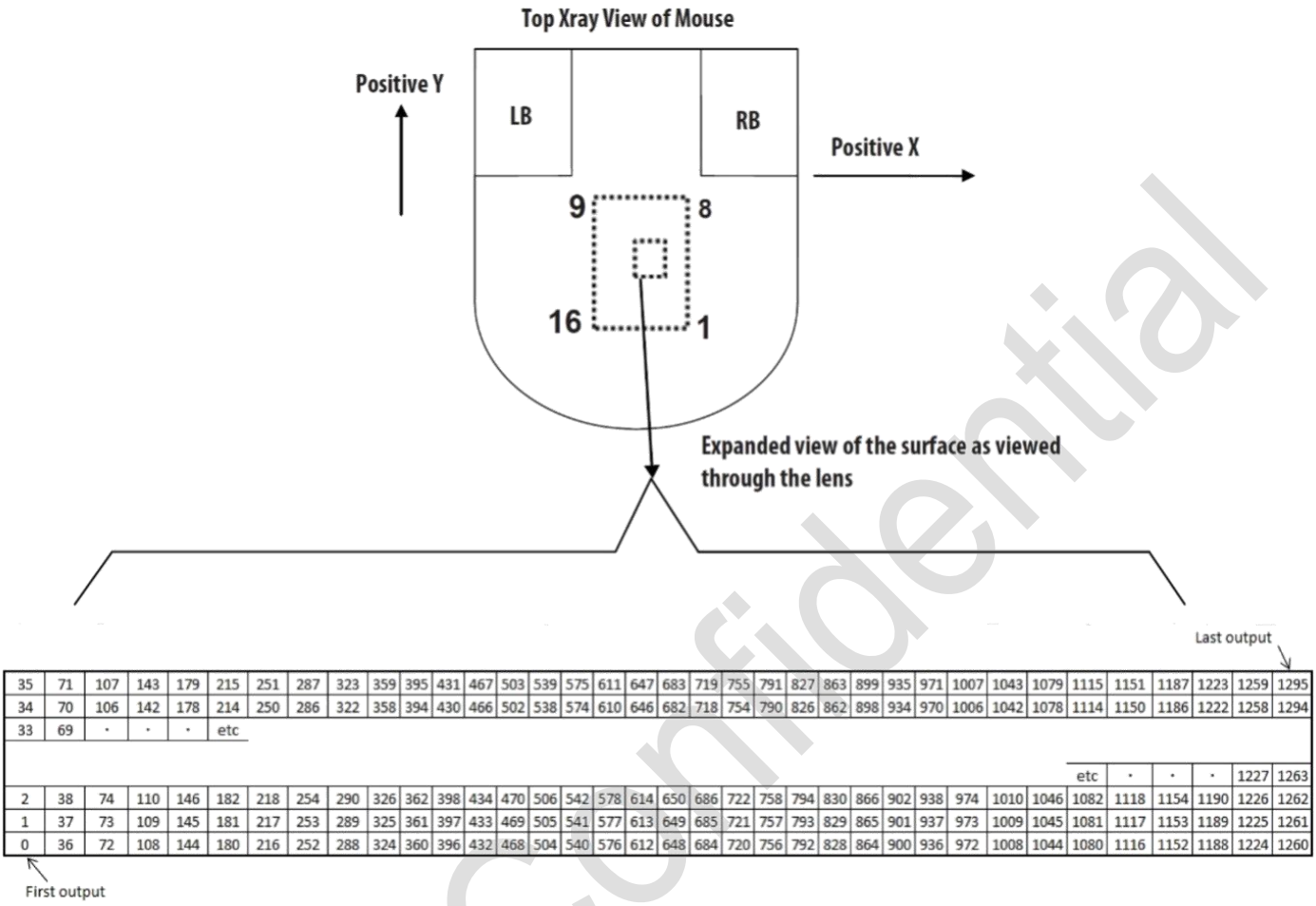
This section describes the method to download a full array of RawData values.

In order to trigger the RawData output, write to the *RawData_Grab* register. The 1 element of RawData is retrieved by reading the *RAWDATA_GRAB* register using register read method after *RAWDATA_GRAB_STATUS* register reports *PG_VALID* to be TRUE. During the RawData output process, it is a MUST to place the mouse at stationary position.

RawData output procedure:

1. The chip should be powered up and reset correctly.
2. Write register 0x7F with value 0x00
3. Write register 0x40 with value 0x80
4. Continuously read register 0x02 (Motion) until getting both *OP_Mode1* and *OP_Mode0* equal to 0.
5. Write register 0x50 with value 0x01
6. Write register 0x55 with value 0x04
7. Write register 0x58 with value 0xFF
8. Continuously read register 0x59 until getting both *PG_FIRST* and *PG_VALID* as "1"
9. Read the first rawdata from register 0x58
10. Continuously read register 0x59 until getting *PG_VALID* is "1".
11. Read register 0x58 for 7 bits ADC data (*RAWDATA* 6-0). Repeat (10) and (11) for 1295 times to form a complete picture element array information.
12. Write register 0x40 with value 0x00
13. Write register 0x50 with value 0x00
14. Write register 0x55 with value 0x00

RawData Map



35	71	107	143	179	215	251	287	323	359	395	431	467	503	539	575	611	647	683	719	755	791	827	863	899	935	971	1007	1043	1079	1115	1151	1187	1223	1259	1295
34	70	106	142	178	214	250	286	322	358	394	430	466	502	538	574	610	646	682	718	754	790	826	862	898	934	970	1006	1042	1078	1114	1150	1186	1222	1258	1294
33	69	·	·	·	etc																														
																														etc	·	·	·	1227	1263
2	38	74	110	146	182	218	254	290	326	362	398	434	470	506	542	578	614	650	686	722	758	794	830	866	902	938	974	1010	1046	1082	1118	1154	1190	1226	1262
1	37	73	109	145	181	217	253	289	325	361	397	433	469	505	541	577	613	649	685	721	757	793	829	865	901	937	973	1009	1045	1081	1117	1153	1189	1225	1261
0	36	72	108	144	180	216	252	288	324	360	396	432	468	504	540	576	612	648	684	720	756	792	828	864	900	936	972	1008	1044	1080	1116	1152	1188	1224	1260

Figure 17. RawData Map (Surface Referenced)

7.2 Shutdown

The chip can be set in Shutdown mode by writing to the Shutdown register 0x3B with value 0xB6. The SPI port should not be accessed when Shutdown mode is asserted except the power-up command (writing 0x5A to register 0x3A). Other ICs on the same SPI bus can be accessed so long as the chip's NCS pin is not asserted.

To de-assert Shutdown mode, please perform Power-Up sequence from step 2.

Table 10. Pin Status in Shutdown Mode

Pin	Status
NRESET	High
NCS	High*[1]
MISO	Hi-Z*[2]
SCLK	Ignore if NCS = 1*[3]
MOSI	Ignore if NCS = 1*[4]
MOTION	Output High

Notes: *

1. NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Shutdown unless powering up the Chip. It must be held to 0 (low) if the chip is to be re-powered up from shutdown (writing 0x5A to register 0x3a).
2. MISO should be pulled up during shutdown in order to meet the low power consumption specification in the datasheet.
3. SCLK is ignored if NCS is 1 (high). It is functional if NCS is 0 (low).
4. MOSI is ignored if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5A to register 0x3A).

CAUTION: There is long wakeup time from shutdown. Shutdown should not be used for power management during normal mouse motion.

7.3 Gaming and Office Mode Setting

The chip can be programmed to different gaming and office modes per the register settings in the table below. Please note that upon chip start-up per the recommended Power-Up Sequence, the chip is set to High Performance Mode as default.

High Performance Mode (Default)	Low Power Mode	Office Mode
write register 0x7F with value 0x05	write register 0x7F with value 0x05	write register 0x7F with value 0x05
write register 0x51 with value 0x40	write register 0x51 with value 0x40	write register 0x51 with value 0x28
write register 0x53 with value 0x40	write register 0x53 with value 0x40	write register 0x53 with value 0x30
write register 0x61 with value 0x31	write register 0x61 with value 0x3B	write register 0x61 with value 0x3B
write register 0x6E with value 0x0F	write register 0x6E with value 0x1F	write register 0x6E with value 0x1F
write register 0x7F with value 0x07	write register 0x7F with value 0x07	write register 0x7F with value 0x07
write register 0x42 with value 0x32	write register 0x42 with value 0x32	write register 0x42 with value 0x32
write register 0x43 with value 0x00	write register 0x43 with value 0x00	write register 0x43 with value 0x00
write register 0x7F with value 0x0D	write register 0x7F with value 0x0D	write register 0x7F with value 0x0D
write register 0x51 with value 0x00	write register 0x51 with value 0x00	write register 0x51 with value 0x00
write register 0x52 with value 0x49	write register 0x52 with value 0x49	write register 0x52 with value 0x49
write register 0x53 with value 0x00	write register 0x53 with value 0x00	write register 0x53 with value 0x00
write register 0x54 with value 0x5B	write register 0x54 with value 0x5B	write register 0x54 with value 0x5B
write register 0x55 with value 0x00	write register 0x55 with value 0x00	write register 0x55 with value 0x00
write register 0x56 with value 0x64	write register 0x56 with value 0x64	write register 0x56 with value 0x64
write register 0x57 with value 0x02	write register 0x57 with value 0x02	write register 0x57 with value 0x02
write register 0x58 with value 0xA5	write register 0x58 with value 0xA5	write register 0x58 with value 0xA5
write register 0x7F with value 0x00	write register 0x7F with value 0x00	write register 0x7F with value 0x00
write register 0x54 with value 0x54	write register 0x54 with value 0x54	write register 0x54 with value 0x52
write register 0x78 with value 0x01	write register 0x78 with value 0x01	write register 0x78 with value 0x0A
write register 0x79 with value 0x9C	write register 0x79 with value 0x9C	write register 0x79 with value 0x0F
write register 0x40 bit[1:0] with value 0x0	write register 0x40 bit[1:0] with value 0x1	write register 0x40 bit[1:0] with value 0x02

Note:

Special precaution needs to be taken for register 0x40 to avoid overwrite other bits in the register. When writing the bit[1:0] to configure to different modes, one need to read and store its current value first, then apply bit masking and write back the new value into the register. Refer to section 8.3 for the detail.

Corded Gaming Mode
write register 0x7F with value 0x05
write register 0x51 with value 0x40
write register 0x53 with value 0x40
write register 0x61 with value 0x31
write register 0x6E with value 0x0F
write register 0x7F with value 0x07
write register 0x42 with value 0x2F
write register 0x43 with value 0x00
write register 0x7F with value 0x0D
write register 0x51 with value 0x12
write register 0x52 with value 0xDB
write register 0x53 with value 0x12
write register 0x54 with value 0xDC
write register 0x55 with value 0x12
write register 0x56 with value 0xEA
write register 0x57 with value 0x15
write register 0x58 with value 0x2D
write register 0x7F with value 0x00
write register 0x54 with value 0x55
write register 0x40 with value 0x83

7.4 Universal Lift Cut Off

The chip provides 1mm and 2mm universal lift cut off setting and the setting applies to all mats, refer to *LIFT_CONFIG* register for the detail of lift cut off setting configuration. Upon ship start-up per the recommended Power-Up sequence in the datasheet, the chip is set to 1mm lift cut off setting as default.

7.5 Manual Lift Cut Off Calibration

The chip has the capability to optimize its lift performance by tuning parameters on a specific gaming mat or tracking surface, this feature involves end user interaction.

7.5.1 Lift Cut off Calibration Procedures

1. Ensured that the chip is powered up according to the Power-Up Sequence in section 6.1.

2. Prompt the user that the manual lift cut off calibration is about to begin and ensure that the mouse is placed nominally on the surface (mouse is not lifted).

3. Start the calibration procedure by loading the following register values in sequence.
   a. Write register 0x7F with value 0x00
   b. Read register 0x40 and store its value into Var_Mode
   c. Write register 0x40 with value 0x80
   d. Write register 0x7F with value 0x05
   e. Write register 0x43 with value 0xE7
   f. Write register 0x7F with value 0x04
   g. Write register 0x40 with value 0xC0
   h. Write register 0x41 with value 0x10
   i. Write register 0x44 with value 0x0C
   j. Write register 0x45 with value 0x0C
   k. Write register 0x46 with value 0x0C
   l. Write register 0x47with value 0x0C
   m. Write register 0x48 with value 0x0C
   n. Write register 0x49 with value 0x0C
   o. Write register 0x4A with value 0x0C
   p. Write register 0x4B with value 0x0C
   q. Write register 0x40 with value 0xC1

4. The calibration procedure can be started by a SW prompt to the user or user-initiated through a mouse-click event. Recommend to move the mouse over a distance of >20inch to cover most area of the mat.

5. Write register 0x40 with value 0x40 to stop the calibration process.

6. Continuously read register 0x4C bit[3:0] to check the status of the calibration process.

If returned value equals to 5 indicates the calibration is successful. Calibration can proceed to the next step or continue until user initiates a mouse-click event.

Else, the calibration is failed, load the following register values to return back to Universal 1mm setting and the calibration process need to be restarted from step 2.

   a. Write register 0x4E with value 0x08
   b. Write register 0x7F with value 0x05
   c. Write register 0x43 with value 0xE4
   d. Write register 0x7F with value 0x00
   e. Write register 0x40 with Var_Mode

7. Write the following set of register values in sequence if the calibration is successful,
   a. Read register 0x4D and store its value into VarA
   b. Write register 0x7F with value 0x0C
   c. Store value 0x0C into VarB
   d. Store value 0x30 into VarC
   e. Write register 0x4E with value 0x08
   f. Write register 0x7F with value 0x05
   g. Write register 0x43 with value 0xE4
   h. Write register 0x7F with value 0x00
   i. Write register 0x40 with Var_Mode
8. Perform the Firmware Aided Manual Calibration, refer to section 7.5.2. **(Optional)**
9. Prompt the user that the calibration process is completed, continue to section 7.5.3 to enable Lift Cut off Calibration Register Setting.

7.5.1.1 Firmware Aided Manual Lift Cut Off Calibration

Firmware Aided Manual Lift Cut Off Calibration provides additional steps to ensure manual calibration that provides good tracking with lift cut off height of approximately 1.2mm on unique surface. This section is optional and is not necessarily required to successfully complete the manual calibration in section 7.5.1. It will not impact lift cut off performance for other surfaces.

Procedures:

1. While the mouse is being moved on the surface, continuously read and accumulate the values of SQUAL, *RawData_Sum* and *SQUAL2* registers in burst mode operation. After accumulating at least 3000 set of samples, calculate the average value for each register and store the average values into *Var_SQUAL_Avg*, *Var_RawData_Sum_Avg*, and *Var_SQUAL2_Avg* respectively.

   Motion Burst Report order:

   BYTE[00] = Motion
   BYTE[01] = Observation
   BYTE[02] = Delta_X_L
   BYTE[03] = Delta_X_H
   BYTE[04] = Delta_Y_L
   BYTE[05] = Delta_Y_H
   BYTE[06] = SQUAL
   BYTE[07] = RawData_Sum
   BYTE[08] = Maximum_RawData
   BYTE[09] = Minimum_Rawdata
   BYTE[10] = Shutter_Upper
   BYTE[11] = Shutter_Lower
   BYTE[12] = Reserved
   BYTE[13] = Reserved
   BYTE[14] = SQUAL2

Note:

   a. Recommend to assign 32-bit unsigned integer for the accumulators to prevent data overflow.
   b. Refer to section 5.8 for the detail of Burst Mode Operation.

2. Check *RawData_Sum_Avg*:

   If (*RawData_Sum_Avg* < 48), store value 23 into *Var_Squal_TH*.

   Else, store value 30 into *Var_Squal_TH*

3. Calculate the SQUAL ratio and store into *Var_SQUAL_Ratio*:

   Var_SQUAL_Ratio = (*Var_SQUAL2_Avg x* 100)/*Var_SQUAL_Avg*

4. Check *Var_SQUAL_Ratio* and *RawData_Sum_Avg*:

   If ((*Var_SQUAL_ratio* < *Var_Squal_TH*) && (*RawData_Sum_Avg* < 68)),

   unique surface is detected, store value 0x25 into VarA, store value 0x0C into VarB and store 0x2D into VarC.

   Else, **unique surface is not detected,** no change to VarA, VarB and VarC.

7.5.2 Enable Lift Cut off Calibration Register Setting

Write the following set of register values to enable the lift cut off calibration register setting on a specific gaming mat. VarA, VarB and VarC obtained from the section 7.5.1 would be used in this section.

1. Write register 0x7F with value 0x0C
2. Write register 0x41 with **VarA**
3. Write register 0x43 with **VarC**
4. Write register 0x44 with **VarB**
5. Write register 0x4E with value 0x08
6. Write register 0x5A with value 0x0D
7. Write register 0x5B with value 0x05
8. Write register 0x7F with value 0x05
9. Write register 0x6E with value 0x0F
10. Write register 0x7F with value 0x09
11. Write register 0x71 with value 0x0C
12. Write register 0x7F with value 0x00

7.5.3 Disable Lift Cut off Calibration Register Setting

Write the following set of register values to disable lift cut off calibration register setting in Section 7.5.2 and revert to default universal 1 mm lift cut off setting.

1. Write register 0x7F with value 0x0C
2. Write register 0x41 with value 0x25
3. Write register 0x43 with value 0x2D
4. Write register 0x44 with value 0x0C
5. Write register 0x4A with value 0x10
6. Write register 0x4B with value 0x0C
7. Write register 0x4C with value 0x40
8. Write register 0x4E with value 0x08
9. Write register 0x53 with value 0x16
10. Write register 0x54 with value 0x1A
11. Write register 0x55 with value 0x18
12. Write register 0x56 with value 0x14
13. Write register 0x5A with value 0x0D
14. Write register 0x5B with value 0x05
15. Write register 0x5F with value 0x1E
16. Write register 0x66 with value 0x30
17. Write register 0x7F with value 0x05
18. Write register 0x6E with value 0x0F
19. Write register 0x7F with value 0x09
20. Write register 0x71 with value 0x0C
21. Write register 0x72 with value 0x07
22. Write register 0x7F with value 0x00

7.6 Power Management for Wireless Mode

The chip has three power saving modes. Each mode has a different motion detection period with its respective response time to mouse motion. Response time is the time taken for the chip to wake up from rest mode when motion is detected. When left idle, the chip automatically changes or downshift from Run mode to Rest1, then to Rest2 and finally to Rest3 which consumes the least amount of current.

The current consumption is lowest at Rest3 and highest at Rest1. However, the time required for the chip to respond to motion from Rest1 is the shortest and longest from Rest3. Downshift time is the elapsed time (under no motion condition) from an existing mode to the next mode. For example, it takes 10s for the chip which is in Rest1 mode to change (downshift) to Rest2 mode. The response time and downshift time for each mode are shown in the following table.

However, user can change the timing setting for each rest mode via register 0x77 through 0x7C.

Table 11. Rest Modes Response and Downshift Time

Rest Mode	HP Mode / LP Mode		Office Mode	
	Response Time	Downshift Time	Response Time	Downshift Time
Rest1	< 2ms	1s	< 20ms	1s
Rest2	< 200ms	10s	< 200ms	10s
Rest3	< 1000ms	600s	< 1000ms	600s

Note: The timings are based on power-up initialization register setting in the section 6.1 and Gaming and Office Mode Setting in the section 7.3. The timings are subjected to change if any of the register 0x77 to 0x7C value is updated.

8.0 Registers

8.1 Registers Summary Table

The chip registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Access	Reset Value	Address	Register	Access	Reset Value
0x00	Product_ID	R	0x51	0x4A	Resolution_Y_Low	R/W	0x63
0x01	Revision_ID	R	0x00	0x4B	Resolution_Y_High	R/W	0x00
0x02	Motion	R/W	0x00	0x56	Angle Snap	R/W	0x0D
0x03	Delta_X_L	R	0x00	0x58	RawData output	R	0x00
0x04	Delta_X_H	R	0x00	0x59	RawData status	R	0x00
0x05	Delta_Y_L	R	0x00	0x5A	Ripple_Control	R/W	0x00
0x06	Delta_Y_H	R	0x00	0x5B	Axis_Control	R/W	0x60
0x07	SQUAL	R	0x00	0x5C	Motion_Ctrl	R/W	0x02
0x08	RawData_Sum	R	0x00	0x5F	Inv_Product_ID	R	0xAE
0x09	Maximum_RawData	R	0x00	0x77	Run_Downshift	R/W	0x14
0x0A	Minimum_RawData	R	0x00	0x78	Rest1_Period	R/W	0x01
0x0B	Shutter_Lower	R	0x00	0x79	Rest1_Downshift	R/W	0x90
0x0C	Shutter_Upper	R	0x01	0x7A	Rest2_Period	R/W	0x19
0x15	Observation	R/W	0x80	0x7B	Rest2_Downshift	R/W	0x5E
0x16	Motion_Burst	R/W	0x00	0x7C	Rest3_Period	R/W	0x3F
0x3A	Power_Up_Reset	W	N/A	0x7D	Run_Downshift_Mult	R/W	0x07
0x3B	Shutdown	W	N/A	0x7E	Rest_Downshift_Mult	R/W	0x55
0x40	Performance	R/W	0x00	0x0577*	Angle_Tune1	R/W	0x00
0x47	Set_Resolution	W	0x00	0x0578*	Angle_Tune2	R/W	0x00
0x48	Resolution _X_Low	R/W	0x63	0x0C4E*	Lift_Config	R/W	0x08
0x49	Resolution _X_High	R/W	0x00				

Note:

1. R = Read, W = Write, Read/Write= RW
2. * - In order to access the register:
   a. Write register 0x7F with the value of MSB(byte) in the address.
   b. Read/Write the register value with the lower byte address.
   c. Write register 0x7F with the value 0x00.
3. Eg: To write register 0x0C4E (*Lift_Config*) with value 0x01
   a. Write register 0x7F with value 0x0C,
   b. Write register 0x4E with value 0x01,
   c. Write register 0x7F with value 0x00

8.2 Registers Description

Register Name	PRODUCT_ID							
Bank	-			Address		0x00		
Access	R			Default Value		0x51		
Bit	7	6	5	4	3	2	1	0
Field	PID [7:0]							
Description	This register contains a unique identification assigned to the chip. The value in this register does not change, it can be used to verify that the serial communications link is functional.							

Register Name	REVISION_ID							
Bank	-			Address		0x01		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	REV [7:0]							
Description	This register contains the current IC revision.							

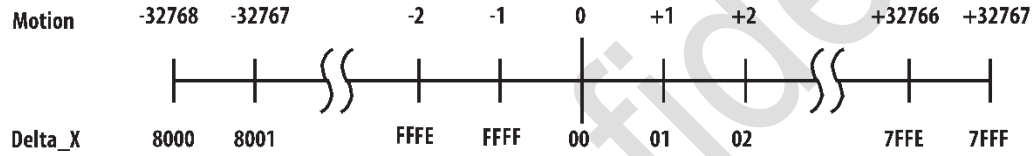
Register Name	MOTION							
Bank	-			**Address**		0x02		
Access	R			**Default Value**		0x00		
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	MOT	Reserved	Reserved	Reserved	Lift_Stat	Reserved	OP_Mode1	OP_Mode0
Description	This register allows the user to determine if motion has occurred since the last time it was read. The procedure to read the motion registers (*Delta_X_L, Delta_X_H, Delta_Y_L* and *Delta_Y_H*) is as follows: 1. Read the Motion register. This will freeze the *Delta_X_L, Delta_X_H, Delta_Y_L* and *Delta_Y_H* register values. 2. If the MOT bit is set, *Delta_X_L, Delta_X_H, Delta_Y_L* and *Delta_Y_H* registers should be read in the given sequence to get the accumulated motion. 3. To read a new set of motion data (*Delta_X_L, Delta_X_H, Delta_Y_L* and *Delta_Y_H*), repeat from Step 1. Write any value to this register will clear all motion data. Note: if *Delta_X_L, Delta_X_H, Delta_Y_L* and *Delta_Y_H* registers are not read before the motion register is read for the second time, the data in *Delta_X_L, Delta_X_H, Delta_Y_L* and *Delta_Y_H* will be lost.							

Bit Field	Name	Default Value	Description
7	MOT	0	Motion since last report 0: No motion 1: Motion occurred, data ready for reading in *Delta_X_L, Delta_X_H, Delta_Y_L* and *Delta_Y_H* registers
3	Lift_Stat	0	Indicate the lift status of chip 0: Chip on surface 1: Chip lifted
1:0	OP_Mode[1:0]	0	0: Run Mode 1: Rest 1 Mode 2: Rest 2 Mode 3: Rest 3 Mode

Register Name	DELTA_X_L							
Bank	-			Address		0x03		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	X7	X6	X5	X4	X3	X2	X1	X0
Register Name	DELTA_X_H							
Bank	-			Address		0x04		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	X15	X14	X13	X12	X11	X10	X9	X8

Description

Upper 8 bits is *Delta_X_H and* Lower 8 bits is *Delta_X_L*.
Overall *Delta_X* is 16 bits 2's complement number.
X movement is counts since last report. Absolute value is determined by resolution.

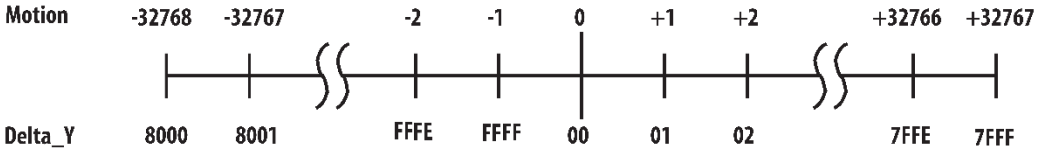


The *Delta_X_L* need to be read first follow by *Delta_X_H* to have the full motion data.
Note: It is recommended that register 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.

Register Name	DELTA_Y_L							
Bank	-			Address		0x05		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Register Name	DELTA_Y_H							
Bank	-			Address		0x06		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8

Description

Upper 8 bits is *Delta_Y_H and* Lower 8 bits is *Delta_Y_L*.
Overall *Delta_Y* is 16 bits 2's complement number.
Y movement is counts since last report. Absolute value is determined by resolution.



The *Delta_Y_L* need to be read first follow by *Delta_Y_H* to have the full motion data.
Note: It is recommended that register 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.

Register Name	SQUAL							
Bank	-			Address		0x07		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	SQ7	SQ6	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0
Description	The SQUAL (Surface quality) register is a measure of the number of valid features visible by the chip in the current frame. Use the following formula to find the total number of valid features. Number of Features = *SQUAL* Register Value x 4 The maximum *SQUAL* register value is 0xB6. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface is expected. SQUAL values are only valid when chip is in run mode. Disable Rest mode before measuring SQUAL.							

Register Name	RAWDATA_SUM							
Bank	-			Address		0x08		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RDS7	RDS6	RDS5	RDS4	RDS3	RDS2	RDS1	RDS0
Description	This register is used to find the chip average rawdata value. It reports the upper byte of an 18-bit counter which sums all 1296 rawdata in the current frame. To find the average rawdata value follows the formula below: Average pixel value = PIX_ACCUM x 1024/1296 The maximum register value is 0xA0 (hex) or 160 (dec) and the minimum register value is 0. The data sum value can change every frame. Disable rest mode before reading *RawData_sum* value.							

Register Name	MAXIMUM_RAWDATA							
Bank	-			Address		0x09		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	MaxRD7	MaxRD6	MaxRD5	MaxRD4	MaxRD3	MaxRD2	MaxRD1	MaxRD0
Description	Maximum RawData value in current frame. Minimum value = 0, maximum value = 127. The maximum rawdata value can change every frame.							

Register Name	MINIMUM_RAWDATA							
Bank	-			Address		0x0A		
Access	R			Default Value		0x7F		
Bit	7	6	5	4	3	2	1	0
Field	MinRD7	MinRD6	MinRD5	MinRD4	MinRD3	MinRD2	MinRD1	MinRD0
Description	Minimum RawData value in current frame. Minimum value = 0, maximum value = 127. The minimum rawdata value can change every frame.							

Register Name	SHUTTER_LOWER							
Bank	-			Address		0x0B		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	S7	S6	S5	S4	S3	S2	S1	S0
Register Name	SHUTTER_UPPER							
Bank	-			Address		0x0C		
Access	R			Default Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	S11	S10	S9	S8
Description	*SHUTTER_LOWER* is the lower 8-bit and *SHUTTER_UPPER* is the upper 4-bit of the 12-bit *Shutter* register. Read *Shutter_Upper* first, then *Shutter_Lower* consecutively. The shutter is adjusted to keep the average rawdata values within normal operating ranges. The shutter value is checked and automatically adjusted to a new value if needed on every frame when operating in default mode. The shutter unit is the clock cycles of the internal oscillator (nominal 68MHz).							

Register Name	CHIP_OBSERVATION							
Bank	-			Address		0x15		
Access	R			Default Value		0x80		
Bit	7	6	5	4	3	2	1	0
Field	CO7	CO6	CO5	CO4	CO3	CO2	CO1	CO0
Description	The user must clear the register by writing 0x00, wait for a minimum Tdly_obs ms & read the register. If the chip is working correctly, the register value of CHIP_OBSERVATION should be 0xB7 or 0xBF. The register may be used as part of recovery scheme to detect a problem caused by EFT/B or ESD event. T_{dly_obs} is defined as the longest frame period + 10% variation. The longest frame period is when chip is in Rest3 mode. Clock frequency tolerance value need to be considered. For example, if the default Rest3 period of 500ms is used, then T_{dly_obs} = 500ms + 50ms							

Register Name	BURST_MOTION_READ							
Bank	-			Address		0x16		
Access	R			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Description	The *Burst_Motion_Read* register is used for high-speed access to the Motion, Observation, *Delta_X_L, Delta_X_H, Delta_Y_L, Delta_Y_H, SQUAL, RawData_Sum, Maximum_RawData, Minimum_RawData, Shutter_Upper* and *Shutter_Lower* registers. Refer section 5.7 for more detail.							

Register Name	POWER_UP_RESET							
Bank	-			Address		0x3A		
Access	R			Default Value		N/A		
Bit	7	6	5	4	3	2	1	0
Field	PRST7	PRST6	PRST5	PRST4	PRST3	PRST2	PRST1	PRST0
Description	Write 0x5A to this register to reset the chip and all settings will revert to default values. Reset is required after recovering from Shutdown mode.							

Register Name	SHUTDOWN							
Bank	-			Address		0x3B		
Access	R			Default Value		N/A		
Bit	7	6	5	4	3	2	1	0
Field	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Description	Write 0xB6 to set the chip to Shutdown mode. Refer section 7.2 for more details on recovery procedure.							

Register Name	PERFORMANCE							
Bank	-			Address		0x40		
Access	R/W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AWAKE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Description	This register configures the operating mode of the chip.							

Bit Field	Name	Default Value	Description
7	AWAKE	0	0: Enable Rest Mode 1: Disable Rest Mode

Register Name	SET_RESOLUTION							
Bank	-			Address		0x47		
Access	W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SET_RES
Description	After update the resolution setting, either in *RESOLUTION_X* or/and *RESOLUTION_Y*, write value 0x01 into *SET_RESOLUTION* for the chip to use the new resolution setting.							

Bit Field	Name	Default Value	Description
0	SET_RES	0	1: update resolution setting

Register Name	RESOLUTION_X_LOW							
Bank	-			Address		0x48		
Access	R/W			Default Value		0x63		
Bit	7	6	5	4	3	2	1	0
Field	RESX7	RESX6	RESX5	RESX4	RESX3	RESX2	RESX1	RESX0
Register Name	**RESOLUTION_X_HIGH**							
Bank	-			Address		0x49		
Access	R/W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RESX15	RESX14	RESX13	RESX12	RESX11	RESX10	RESX9	RESX8

Description

This register allows to change the resolution of X-axis of the chip.
RESOLUTION_X_LOW is the lower 8-bit and *RESOLUTION _X_HIGH* is the upper 8-bit of 16-bit *RESOLUTION_X* register.
Write to *RESOLUTION_X_LOW* first, then *RESOLUTION_X_HIGH* consecutively.

Set X-axis Resolution:
0x0000: 50CPI
0x0001: 100CPI
0x0002: 150CPI
:
0x0063: 5000CPI (Default)
:
0x018F: 20000CPI
:
0x0207: 26000CPI (max)

After update the resolution setting, either in *RESOLUTION_X* or/and *RESOLUTION_Y*, write value 0x01 into *SET_RESOLUTION* for the chip to use the new resolution setting.

Note: It is recommended to set bit-7 in *RIPPLE_CONTROL* register to enable the ripple control when select 9000 CPI and above.

Register Name	RESOLUTION_Y_LOW							
Bank	-			Address		0x4A		
Access	R/W			Default Value		0x63		
Bit	7	6	5	4	3	2	1	0
Field	RESY7	RESY6	RESY5	RESY4	RESY3	RESY2	RESY1	RESY0
Register Name	RESOLUTION_Y_HIGH							
Bank	-			Address		0x4B		
Access	R/W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RESY15	RESY14	RESY13	RESY12	RESY11	RESY10	RESY9	RESY8

Description

This register allows to change the resolution of Y-axis of the chip.
RESOLUTION_Y_LOW is the lower 8-bit and *RESOLUTION _Y_HIGH* is the upper 8-bit of 16-bit *RESOLUTION_Y* register.
Write to *RESOLUTION_Y_LOW* first, then *RESOLUTION_Y_HIGH* consecutively.

Set Y-axis Resolution:
0x0000: 50CPI
0x0001: 100CPI
0x0002: 150CPI
:
0x0063: 5000CPI (Default)
:
0x018F: 20000CPI
:
0x0207: 26000CPI (max)

After update the resolution setting, either in *RESOLUTION_X* or/and *RESOLUTION_Y*, write value 0x01 into *SET_RESOLUTION* for the chip to use the new resolution setting.
Note: It is recommended to set bit-7 in *RIPPLE_CONTROL* register to enable the ripple control when select 9000 CPI and above.

Register Name	ANGLE_SNAP							
Bank	-			Address		0x56		
Access	R/W			Default Value		0x0D		
Bit	7	6	5	4	3	2	1	0
Field	EN	0	0	0	1	1	0	1

Description Write to this register to enable angle snap feature.

Bit Field	Name	Default Value	Description
7	EN	0	0: Angle snap disable 1: Angle snap enable

Register Name	RAWDATA_GRAB							
Bank	-			Address		0x58		
Access	R/W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RAWDATA7	RAWDATA6	RAWDATA5	RAWDATA4	RAWDATA3	RAWDATA2	RAWDATA1	RAWDATA0
Description	This register contains the rawdata levels when the *RawData Grab* process is enabled. For details of the *RawData Grab* process, please refer to section 7.1.							

Register Name	RAWDATA_GRAB_STATUS							
Bank	-			Address		0x59		
Access	R/W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	PG_VALID	PG_FIRST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Description	Write to this register to enable angle snap feature.							

Bit Field	Name	Default Value	Description
7	PG_VALID	0	1: RawData Grab valid
6	PG_FIRST	0	1: RawData Grab first

Register Name	RIPPLE_CONTROL							
Bank	-			Address		0x5A		
Access	R/W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	CTRL8	Reserved	Reserved	1	Reserved	Reserved	Reserved	Reserved
Description	Write to this register to enable or disable Ripple Control feature. Upon chip start-up per the recommended Power-Up sequence in the section 6.1, Ripple Control is disabled as default.							

Bit Field	Name	Default Value	Description
7	CTRL8	0	0: Ripple Control disable 1: Ripple Control enable

Register Name	AXIS_CONTROL							
Bank	-			Address		0x5B		
Access	R/W			Default Value		0x60		
Bit	7	6	5	4	3	2	1	0
Field	Swap_XY	INV_Y	INV_X	Reserved	Reserved	Reserved	Reserved	Reserved
Description	The register set the axis direction of the chip reporting							

Bit Field	Name	Default Value	Description
7	Swap_XY	0	1: Swap XY directions
6	INV_Y	1	1: Invert Y direction
5	INV_X	1	1: Invert X direction

Register Name	MOTION_CTRL							
Bank	-			Address		0x5C		
Access	R/W			Default Value		0x02		
Bit	7	6	5	4	3	2	1	0
Field	MOT_Set	Reserved	Reserved	Reserved	Reserved	Reserved	RES_MOD	Reserved
Description	Configures the motion pin setting and select the X-axis and Y-axis resolution mode.							

Bit Field	Name	Default Value	Description
7	MOT_Set	0	0: motion active low (default) 1: motion active high
2	RES_Mod	1	0: Both X-axis and Y-axis resolution are defined by *RESOLUTION_X_LOW* and *RESOLUTION_X_HIGH* 1: X-axis resolution is defined by *RESOLUTION_X_LOW* and *RESOLUTION_X_HIGH* and Y-axis resolution is defined by *RESOLUION_Y_LOW* and *RESOLUION_Y_HIGH* (default)

Register Name	INV_PROD_ID							
Bank	-			Address		0x5F		
Access	R/W			Default Value		0xAE		
Bit	7	6	5	4	3	2	1	0
Field	IPID [7:0]							
Description	This register value is the inverse of the *Product_ID* register value. It is used to test the SPI port hardware.							

Register Name	RUN_DOWNSHIFT							
Bank	-			Address		0x77		
Access	R/W			Default Value		0x14		
Bit	7	6	5	4	3	2	1	0
Field	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Description	This register set the Run to Rest1 downshift time. Use the formula below for calculation. Run Downshift time (ms) = *RUN_DOWNSHIFT*[7:0] x *RUN_DOWNSHIFT_MULT* (default 256) x 50µs Upon Chip start-up per the recommended Power-Up Sequence, *RUN_DOWNSHIFT* is set to 1s as default. Default Run Downshift = 79(0x4F) x 256 x 50µs = 1s Min value is 0x01. A value of 0x00 will be internally clipped to 0x01. All the above values are expected to have ± 10% tolerance.							

Register Name	REST1_PERIOD							
Bank	-			Address		0x78		
Access	R/W			Default Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	R1R7	R1R6	R1R5	R1R4	R1R3	R1R2	R1R1	R1R0
Description	This register set the Rest1 period. Rest1 period = *REST1_PERIOD*[7:0] x 1ms Upon Chip start-up per the recommended Power-Up Sequence, *REST1_PERIOD* is set to 1ms as default. Default Rest1 period = 1(0x01) x 1ms = 1ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have ± 10% tolerance.							

Register Name	REST1_DOWNSHIFT							
Bank	-			Address		0x79		
Access	R/W			Default Value		0x90		
Bit	7	6	5	4	3	2	1	0
Field	R1D7	R1D6	R1D5	R1D4	R1D3	R1D2	R1D1	R1D0
Description	This register set the Rest1 to Rest2 downshift time. Use the formula below for calculation. Rest1 Downshift time (ms) = *REST1_DOWNSHIFT*[7:0] x *REST1_DOWNSHIFT_MULT* (default 64) x *REST1* period (default 1ms) Upon Chip start-up per the recommended Power-Up Sequence, *REST1_DOWNSHIFT* is set to 10s as default. Default = 156(0x9C) x 64 x 1ms = 9984ms = 10s Min value is 0x01. A value of 0x00 will be internally clipped to 0x01. All the above values are expected to have ± 10% tolerance.							

Register Name	REST2_PERIOD							
Bank	-			Address		0x7A		
Access	R/W			Default Value		0x19		
Bit	7	6	5	4	3	2	1	0
Field	R2P7	R2P6	R2P5	R2P4	R2P3	R2P2	R2P1	R2P0
Description	This register set the Rest2 period. Rest2 period = *Rest2_Period*[7:0] x slow clock (1ms) x 4 Upon Chip start-up per the recommended Power-Up Sequence, *REST2_PERIOD* is set to 100ms as default. Default Rest2 period = 25 (0x19) x 1ms x 4= 100ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have ± 10% tolerance.							

Register Name	REST2_DOWNSHIFT							
Bank	-			Address		0x7B		
Access	R/W			Default Value		0x5E		
Bit	7	6	5	4	3	2	1	0
Field	R2D7	R2D6	R2D5	R2D4	R2D3	R2D2	R2D1	R2D0
Description	This register set the Rest2 to Rest3 downshift time. Use the formula below for calculation. Rest2 Downshift time (ms) = *Rest2_Downshit*[7:0] x *REST2_DOWNSHIFT_MULT* (default 64) x rest2_period (default 100ms) Upon Chip start-up per the recommended Power-Up Sequence, Rest2 Downshift time is set to 10 minutes as default. Default = 94(0x5E) x 64 x 100ms = 601.6s = 10min Min value is 0x01. A value of 0x00 will be internally clipped to 0x01. All the above values are expected to have ± 10% tolerance.							

Register Name	REST3_PERIOD							
Bank	-			Address		0x7C		
Access	R/W			Default Value		0x3F		
Bit	7	6	5	4	3	2	1	0
Field	R3P7	R3P6	R3P5	R3P4	R3P3	R3P2	R3P1	R3P0
Description	This register set the Rest3 period. *Rest3 period* = *Rest3_Period*[7:0] x slow clock (1ms) x 8 Upon Chip start-up per the recommended Power-Up Sequence, *Rest3 period* is set to 504ms as default. Default Rest3 period = 63(0x3F) x 1ms x 8 = 504ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have ± 10% tolerance.							

Register Name	RUN_DOWNSHIFT_MULT							
Bank	-			Address		0x7D		
Access	R/W			Default Value		0x07		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	RUN_M3	RUN_M2	RUN_M1	RUN_M0
Description	This register set the Run Downshift Multiplier. (Refer to the formula in Register *RUN_DOWNSHIFT* for the detail)							

Bit Field	Name	Default Value	Description
3:0	RUN_M[3:0]	7	Register value for RUN_DOWNSHIFT_MULT 0: 2 1: 4 2: 8 3: 16 4: 32 5: 64 6: 128 7: 256 8: 512 9: 1024 10: 2048

Register Name	REST_DOWNSHIFT_MULT							
Bank	-			Address		0x7E		
Access	R/W			Default Value		0x55		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	REST_M6	REST_M5	REST_M4	Reserved	REST_M2	REST_M1	REST_M0
Description	This register set the REST Downshift Multiplier. (Refer to the formula in Register *REST1_DOWNSHIFT* and *REST2_DOWNSHIFT*)							

Bit Field	Name	Default Value	Description
6:4	REST_M[6:4]	5	Register value for REST2_DOWNSHIFT_MULT 0: 2 1: 4 2: 8 3: 16 4: 32 5: 64 6: 128 7: 256
2:0	REST_M[2:0]	5	Register value for REST1_DOWNSHIFT_MULT 0: 2 1: 4 2: 8 3: 16 4: 32 5: 64 6: 128 7: 256

Register Name	ANGLE_TUNE1							
Bank	-			Address		0x0577		
Access	R/W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	ANGLE7	ANGLE6	ANGLE5	ANGLE4	ANGLE3	ANGLE2	ANGLE1	ANGLE0
Description	This register set the REST Downshift Multiplier. (Refer to the formula in Register *REST1_DOWNSHIFT* and *REST2_DOWNSHIFT*)							

Bit Field	Name	Default Value	Description
7:0	ANGLE[7:0]	0x00	0xE2: -30 degree 0xF6: -10 degree 0x00: 0 degree (default) 0x0F: +15 degree 0x1E: +30 degree

Register Name	ANGLE_TUNE2							
Bank	-			Address		0x0578		
Access	R/W			Default Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Description	Write to this register to enable angle tune feature							

Bit Field	Name	Default Value	Description
7	EN	0	0: Angle tune disable (default) 1: Angle tune enable

Register Name	LIFT_CONFIG							
Bank	-			Address		0x0C4E		
Access	R/W			Default Value		0x08		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	1	Reserved	LIFT1	LIFT0
Description	Write to this register to enable angle tune feature							

Bit Field	Name	Default Value	Description
1:0	LIFT[1:0]	0	0: 1mm setting (default) 2: 2mm setting

8.3 Bit Masks for Register Write

Special precaution needs to be taken for some of the registers have “Reserved” bit. In order to overwrite specific bits in the register, one need to read and store its current value first, then apply bit masking and write back the new value into the register. This is accomplished by using bitwise operators such as AND(&), OR(|), or INVERSE(~).

Example:

To disable the *Rest Mode* in Register 0x40 (set bit-7 to 1)

Read register 0x40 and store in VarA

VarA |= 0x80

Write register 0x40 with value VarA

To enable the *Rest Mode* in Register 0x40 (set bit-7 to 0)

Read register 0x40 and store in VarA

VarA &= ~ 0x80

Write register 0x40 with value VarA

Revision History

Revision Number	Date	Description
0.8	13 Jan 2021	Initial Creation